MT6575 HSPA Smartphone Application Processor Technical Brief

Version: 0.9
Release date: 2012-01-11

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Specifications are subject to change without notice.

Document Revision History

Revision	Date	Author	Description
0.9	2011-09-26	TH Yang	Initial Draft

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1 System Overview

MT6575 is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable 3G (UMTS) smart phone applications. The chip integrates a 1 GHz Cortex-A9 MCU, an ARM1176 MCU and a powerful DSP processor with multimedia capabilities. The MT6575 interfaces to NAND flash memory, 32-bit mobile DDR and LPDDR2 for optimal performance and supports booting from NAND to minimize the overall BOM cost. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays, MMC/SD cards and external Bluetooth, WiLAN and GPS modules.

The Application processor, a Cortex-A9 which includes a NEON multimedia processing engine, offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All while viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration. The multi-standard video accelerator and an advanced audio subsystem are also included to provide advanced multimedia applications and services such as -streaming audio and video, a multitude of decoders and encoders such as H.264 and MPEG-4. Other audio supports include FR, EFR, HR and AMR vocoders, polyphonic ringtones and advanced audio functions such as echo cancellation, hands-free speakerphone operation and noise cancellation.

An ARM1176JZS core, DSP, and 2G and 3G coprocessors provide a powerful modem subsystem capable of supporting Category 8 (7.2 Mbps) HSDPA downlink and Category 6 (5.76 Mbps) HSUPA uplink data rates, as well as Class 12 GPRS and EDGE.

1.1 Platform Features

General

- Smartphone two MCU subsystems architecture
- NAND flash bootloader

AP MCU subsystem

- 1 GHz Cortex-A9 MCU core for applications/MMI
- Integrated NEON multimedia processing engine
- 32KB I-Cache and 32KB D-Cache
- Dedicated 256KB L2 cache
- Supports DVFS from 0.9V to 1.2V

MD MCU subsystem

- 520 MHz ARM1176 + 260 MHz DSP modem cores
- Dedicated 32KB I-Cache and 32KB D-Cache
- 64KB I- and 64KB D- tghtly couple memory
- 96KB L2 tightly couple memory
- Hardware-based 2G and 3G modems

External memory interface

- Supports Mobile-DDR/LPDDR2 up to 512MB per device
- 32-bit data bus width
- Memory clock up to 260 MHz
- Supports self-refresh mode

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- Low-power operation
- Programmable slew rate for memory controller's IO pads
- Supports 2 external memory devices
- Advanced bandwidth arbitration control

Security

- ARM™ TrustZone® Security

Connectivity

- USB2.0 high-speed OTG supporting 15 Tx and 15 Rx endpoints
- USB1.1 full-speed host
- NAND flash controller supporting NAND bootable, iNAND2® and MoviNAND®
- 4 UART for GPS, BT, FM-RDS, modem and debugging interfaces
- IrDA FIR/MIR/SIR
- SPI for external device
- 3 I2C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
- I2S for connection with optional external hi-end audio codec
- GPIOs
- 4 sets of memory card controller supporting SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols
- Dual SIM card interface

Operating conditions

- Core voltage: 1.1V
- Processor DVFS voltage : 0.9V ~ 1.25V
- I/O voltage: 1.8V/2.8V
- Memory: 1.2V/1.8V
- NAND: 1.8V/2.8V
- LCM interface: 1.8V/2.8V
- Clock source: 26 MHz, 32.768 kHz

Package

- Type: TFBGA
- 12.2mm x 12.2mm
- Height: 1.2mm
- Ball count: 537 balls
- Ball pitch: 0.4mm

Misc

- 2 general-purpose DMA channels + 11 dedicated DMA channels
- 7 PWM
- TDMA and WCDMA timers
- 4 advanced GP timers and 3 OS timers
- Watchdog timer

1.2 MODEM Features

■ **Modem**

- Cat. 8 HSDPA (7.2 Mbps)
- Cat. 6 HSUPA (5.76 Mbps)
- 4-band EDGE/4-band 3G
- Class 12 EDGE, SAIC

Audio

- Sampling rates supported: 6kHz to 96kHz
- Sample formats supported: 8-bit/16-bit, Mono/Stereo
- Interfaces supported: DAI, I2S
- 4-band IIR compensation filter to enhance loudspeaker responses
- Proprietary audio post-processing technologies: BesEQ, BesHeadphone, Bes3d, BesLive, BesTS, BesBass, BesLoudness
- Audio encode: AMR-NB, AMR-WB, AAC
- Audio decode: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE

1.3 Multimedia Features

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Display

- Supports landscape or portrait panel resolution up to qHD (960x540)
- Supports 8/9/16/18/24-bit host interface (MIPI DBI)
- Supports 8/9/16/24/32-bit serial interfaces
- Supports 16/18/24-bit RGB interfaces (MIPI DPI)
- MIPI DSI interface (2 data lanes)
- Embedded LCD gamma correction
- Support true colors
- 6 overlay layers with per-pixel alpha channel and gamma table
- Supports spatial dithering
- Supports 32x32 hardware cursor
- Supports NTSC/PAL TV-Out
- Supports side-by-side format output to stereo 3D panel in both portrait and landscape modes
- Supports external HDMI Tx bridget with high-definition 720p video output

Graphics

- OpenGL ES 1.1/2.0 3D graphic accelerator capable of processing 21M tri/sec and max. 650M pixel/sec @WVGA resolution
- OpenVG1.1 vector graphics accelerator
- 2D graphics hardware accelerator
- Hardware PNG/GIF decoder

Image

- Integrated image signal processor supporting 8MP up to 15fps
- Supports electronic image stabilization
- Supports video stabilization
- Supports local contrast enhancement
- Supports preference color adjustment
- Supports noise reduction
- Supports edge enhancement (sharpness)
- Supports face detection and visual tracking
- Supports 2 channel MIPI CSI-2 high-speed camera serial interface
- Supports Xenon flash
- Hardware JPEG decode: baseline/progressive with YUV422/YUV420/JFIF formats with 35M pixel/sec
- Hardware JPEG encoder: baseline coding with 75M pixel/sec

Video

- H.264 decoder: baseline 720p @ 30fps/4Mbps
- H.264 decoder: main/high profile 720p@24fps/2Mbps
- MPEG-4 SP/H.263 decoder: 720p @ 30fps/4Mbps
- MPEG-4 ASP decoder: 720p @ 30fps/4Mbps
- Xvid/Divx decoder: 720p@30fps/4Mbps
- VP8 decoder: 720p@30fps/4Mbps
- MPEG-4 simple/H.263 encoder: 720p @ 30fps/12.5Mbps
- H.264 encoder: baseline HVGA @ 15fps
- VP8 encoder: QVGA@ 15fps

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1.4 General Descriptions

MediaTek MT6575 is a highly integrated 3G system-on-chip (SOC) which incorporates advanced features e.g. HSPA R6 modem, 1 GHz Cortex-A9 CPU, 3D graphics (OpenGL|ES 2.0), 8M camera ISP, mDDR 200 MHz/LPDDR2 266MHz and High-Definition 720p video decoder. MT6575 helps phone manufacturers build high-performance 3G smart phones with PC-like browser, 3D gaming and cinema class home entertainment experiences.

World-leading technology

Based on MediaTek's world-leading mobile chip SOC architecture and 40nm advanced process, the MT6575 is the brand-new generation smart phone SOC integrating MediaTek HSPA R6 modem, 1GHz CPU, 3D graphics and High-Definition 720p video decoder.

Rich in features, high-valued product

To enrich the camera features, MT6575 equips a 8M camera ISP with advanced features e.g. auto focus, anti-handshake, continuous video AF, face detection, burst shot, optical zoom, panorama view and 3D photos.

Incredible browser experience

The 1 GHz Cortex-A9 CPU with NEON multimedia processing engine brings PC-like browser experiences and help accelerate OpenGL|ES 2.0 3D Adobe Flash 10 rendering performance to an unbeatable level.

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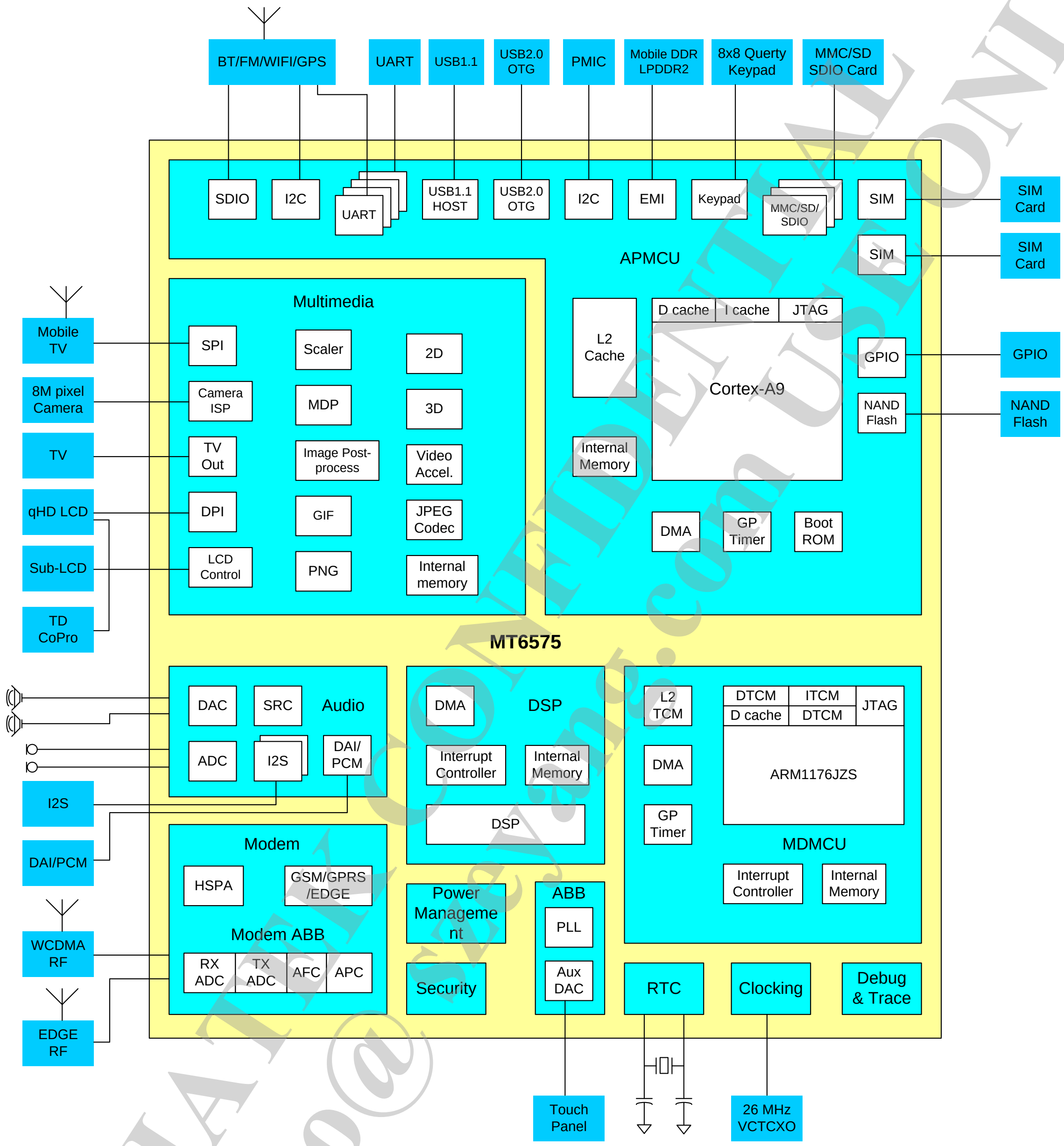

Figure 2-1: Block diagram of MT6575.

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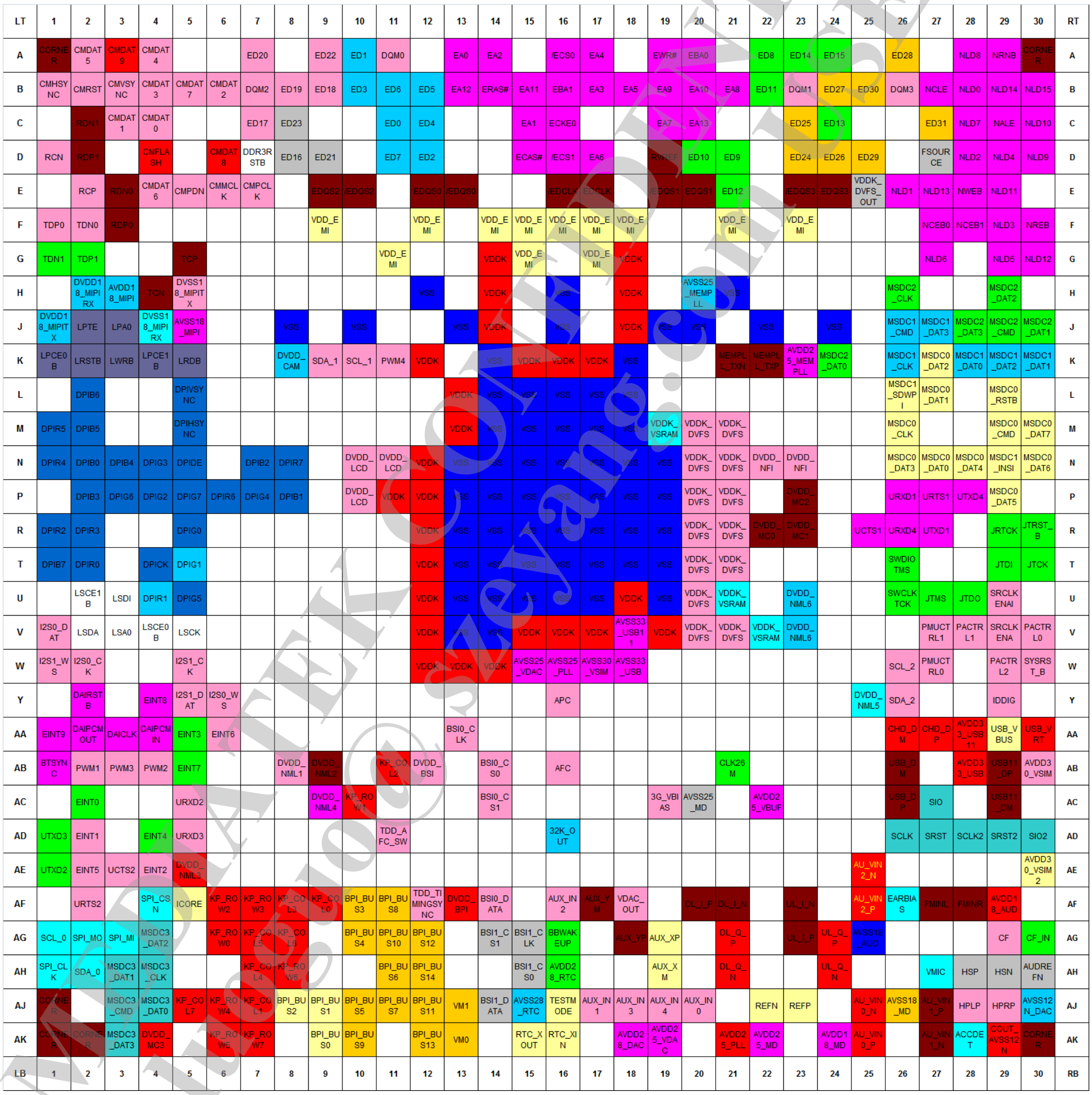
2 Product Description

2.1 Pin Description

2.1.1 Ball Map View



2.1.2 Pin Coordinate

Ball Loc.	Ball Name	Ball Loc.	Ball Name	Ball Loc.	Ball Name
A1	CORNER	AB11	KP_COL2	AJ20	AUX_IN0
B1	CMHSYNC	AD11	TDD_AFC_SW	B21	EA8

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D1	RCN	AF11	BPI_BUS8	D21	ED9
F1	TDP0	AG11	BPI_BUS10	E21	ED12
G1	TDN1	AH11	BPI_BUS6	F21	VDD_EMI
J1	DVDD18_MIPITX	AJ11	BPI_BUS7	H21	VSS
K1	LPCE0B	B12	ED5	K21	MEMPLL_TXN
M1	DPIR5	C12	ED4	M21	VDDK_DVFS
N1	DPIR4	D12	ED2	N21	VDDK_DVFS
R1	DPIR2	E12	EDQS0	P21	VDDK_DVFS
T1	DPIB7	F12	VDD_EMI	R21	VDDK_DVFS
V1	I2S0_DAT	H12	VSS	T21	VDDK_DVFS
W1	I2S1_WS	K12	VDDK	U21	VDDK_VSRAM
AA1	EINT9	N12	VDDK	V21	VDDK_DVFS
AB1	BTSYNC	P12	VDDK	AB21	CLK26M
AD1	UTXD3	R12	VDDK	AF21	DL_I_N
AE1	UTXD2	T12	VDDK	AG21	DL_Q_P
AG1	SCL_0	U12	VDDK	AH21	DL_Q_N
AH1	SPI_CLK	V12	VDDK	AK21	AVDD25_PLL
AJ1	CORNER	W12	VDDK	A22	ED8
AK1	CORNER	AB12	DVDD_BSI	B22	ED11
A2	CMDAT5	AF12	TDD_TIMINGSYNC	J22	VSS
B2	CMRST	AG12	BPI_BUS12	K22	MEMPLL_TXP
C2	RDN1	AH12	BPI_BUS14	N22	DVDD_NFI
D2	RDP1	AJ12	BPI_BUS11	R22	DVDD_MC0
E2	RCP	AK12	BPI_BUS13	V22	VDDK_VSRAM
F2	TDN0	A13	EA0	AC22	AVDD25_VBUF
G2	TDP1	B13	EA12	AJ22	REFN
H2	DVDD18_MIPIRX	E13	/EDQS0	AK22	AVDD25_MD
J2	LPTE	J13	VSS	A23	ED14
K2	LRSTB	L13	VDDK	B23	DQM1
L2	DPIB6	M13	VDDK	C23	ED25
M2	DPIB5	N13	VSS	D23	ED24
N2	DPIB0	P13	VSS	E23	/EDQS3
P2	DPIB3	R13	VSS	F23	VDD_EMI
R2	DPIR3	T13	VSS	K23	AVDD25_MEMPLL
T2	DPIR0	U13	VSS	N23	DVDD_NFI
U2	LSCE1B	V13	VSS	P23	DVDD_MC2
V2	LSDA	W13	VDDK	R23	DVDD_MC1
W2	I2S0_CK	AA13	BSI0_CLK	U23	DVDD_NML6

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Y2	DAIRSTB	AF13	DVDD_BPI	V23	DVDD_NML6
AA2	DAIPCMOUT	AJ13	VM1	AF23	UL_I_N
AB2	PWM1	AK13	VM0	AG23	UL_I_P
AC2	EINT0	A14	EA2	AJ23	REFP
AD2	EINT1	B14	ERAS#	A24	ED15
AE2	EINT5	F14	VDD_EMI	B24	ED27
AF2	URTS2	G14	VDDK	C24	ED13
AG2	SPI_MO	H14	VDDK	D24	ED26
AH2	SDA_0	J14	VDDK	E24	EDQS3
AK2	CORNER	K14	VSS	J24	VSS
A3	CMDAT9	L14	VSS	K24	MSDC2_DAT0
B3	CMVSYNC	M14	VSS	AG24	UL_Q_P
C3	CMDAT1	N14	VSS	AH24	UL_Q_N
E3	RDN0	P14	VSS	AK24	AVDD18_MD
F3	RDP0	R14	VSS	B25	ED30
H3	AVDD18_MIPI	T14	VSS	D25	ED29
J3	LPA0	U14	VSS	E25	VDDK_DVFS_OUT
K3	LWRB	V14	VSS	R25	UCTS1
N3	DPIB4	W14	VDDK	Y25	DVDD_NML5
P3	DPIG6	AB14	BSI0_CS0	AE25	AU_VIN2_N
U3	LSDI	AC14	BSI0_CS1	AF25	AU_VIN2_P
V3	LSA0	AF14	BSI0_DATA	AG25	AVSS18_AUD
AA3	DAICLK	AG14	BSI1_CS1	AJ25	AU_VIN0_N
AB3	PWM3	AJ14	BSI1_DATA	AK25	AU_VIN0_P
AE3	UCTS2	B15	EA11	A26	ED28
AG3	SPI_MI	C15	EA1	B26	DQM3
AH3	MSDC3_DAT1	D15	ECAS#	E26	NLD1
AJ3	MSDC3_CMD	F15	VDD_EMI	H26	MSDC2_CLK
AK3	MSDC3_DAT3	G15	VDD_EMI	J26	MSDC1_CMD
A4	CMDAT4	K15	VDDK	K26	MSDC1_CLK
B4	CMDAT3	L15	VSS	L26	MSDC1_SDWPI
C4	CMDAT0	M15	VSS	M26	MSDC0_CLK
D4	CMFLASH	N15	VSS	N26	MSDC0_DAT3
E4	CMDAT6	P15	VSS	P26	URXD1
H4	TCN	R15	VSS	R26	URXD4
J4	DVSS18_MIPIRX	T15	VSS	T26	SWDIOTMS
K4	LPCE1B	U15	VSS	U26	SWCLKTCK
N4	DPIG3	V15	VDDK	W26	SCL_2

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P4	DPIG2	W15	AVSS25_VDAC	Y26	SDA_2
T4	DPICK	AG15	BSI1_CLK	AA26	CHD_DM
U4	DPIR1	AH15	BSI1_CS0	AB26	USB_DM
V4	LSCE0B	AJ15	AVSS28_RTC	AC26	USB_DP
Y4	EINT8	AK15	RTC_XOUT	AD26	SCLK
AA4	DAIPCMIN	A16	/ECS0	AF26	EARBIAS
AB4	PWM2	B16	EBA1	AJ26	AVSS18_MD
AD4	EINT4	C16	ECKE0	B27	NCLE
AE4	EINT2	D16	/ECS1	C27	ED31
AF4	SPI_CSN	E16	/EDCLK	D27	FSOURCE
AG4	MSDC3_DAT2	F16	VDD_EMI	E27	NLD13
AH4	MSDC3_CLK	H16	VSS	F27	NCEB0
AJ4	MSDC3_DAT0	J16	VSS	G27	NLD6
AK4	DVDD_MC3	K16	VDDK	J27	MSDC1_DAT3
B5	CMDAT7	L16	VSS	K27	MSDC0_DAT2
E5	CMPDN	M16	VSS	L27	MSDC0_DAT1
G5	TCP	N16	VSS	N27	MSDC0_DAT0
H5	DVSS18_MIPITX	P16	VSS	P27	URTS1
J5	AVSS18_MIPI	R16	VSS	R27	UTXD1
K5	LRDB	T16	VSS	U27	JTMS
L5	DPIVSYNC	U16	VSS	V27	PMUCTRL1
M5	DPIHSYNC	V16	VDDK	W27	PMUCTRL0
N5	DPIDE	W16	AVSS25_PLL	AA27	CHD_DP
P5	DPIG7	Y16	APC	AC27	SIO
R5	DPIG0	AB16	AFC	AD27	SRST
T5	DPIG1	AD16	32K_OUT	AF27	FMINL
U5	DPIG5	AF16	AUX_IN2	AH27	VMIC
V5	LSCK	AG16	BBWAKEUP	AJ27	AU_VIN1_P
W5	I2S1_CK	AH16	AVDD28_RTC	AK27	AU_VIN1_N
Y5	I2S1_DAT	AJ16	TESTMODE	A28	NLD8
AA5	EINT3	AK16	RTC_XIN	B28	NLD0
AB5	EINT7	A17	EA4	C28	NLD7
AC5	URXD2	B17	EA3	D28	NLD2
AD5	URXD3	D17	EA6	E28	NWEB
AE5	DVDD_NML3	E17	EDCLK	F28	NCEB1
AF5	ICORE	F17	VDD_EMI	J28	MSDC2_DAT3
AJ5	KP_COL7	G17	VDD_EMI	K28	MSDC1_DAT0
B6	CMDAT2	K17	VDDK	N28	MSDC0_DAT4

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D6	CMDAT8	L17	VSS	P28	UTXD4
E6	CMMCLK	M17	VSS	U28	JTDO
P6	DPIR6	N17	VSS	V28	PACTRL1
Y6	I2S0_WS	P17	VSS	AA28	AVDD33_USB11
AA6	EINT6	R17	VSS	AB28	AVDD33_USB
AF6	KP_ROW2	T17	VSS	AD28	SCLK2
AG6	KP_ROW0	U17	VSS	AF28	FMINR
AJ6	KP_ROW4	V17	VDDK	AH28	HSP
AK6	KP_ROW5	W17	AVSS30_VSIM	AJ28	HPLP
A7	ED20	AF17	AUX_YM	AK28	ACCDET
B7	DQM2	AJ17	AUX_IN1	A29	NRNB
C7	ED17	B18	EA5	B29	NLD14
D7	DDR3RSTB	F18	VDD_EMI	C29	NALE
E7	CMPCLK	G18	VDDK	D29	NLD4
N7	DPIB2	H18	VDDK	E29	NLD11
P7	DPIG4	J18	VDDK	F29	NLD3
AF7	KP_ROW3	K18	VSS	G29	NLD5
AG7	KP_COL5	L18	VSS	H29	MSDC2_DAT2
AH7	KP_COL4	M18	VSS	J29	MSDC2_CMD
AJ7	KP_COL1	N18	VSS	K29	MSDC1_DAT2
AK7	KP_ROW7	P18	VSS	L29	MSDC0_RSTB
B8	ED19	R18	VSS	M29	MSDC0_CMD
C8	ED23	T18	VSS	N29	MSDC1_INSI
D8	ED16	U18	VDDK	P29	MSDC0_DAT5
J8	VSS	V18	AVSS33_USB11	R29	JRTCK
K8	DVDD_CAM	W18	AVSS33_USB	T29	JTDI
N8	DPIR7	AF18	VDAC_OUT	U29	SRCLKENAI
P8	DPIB1	AG18	AUX_YP	V29	SRCLKENA
AB8	DVDD_NML1	AJ18	AUX_IN3	W29	PACTRL2
AF8	KP_COL3	AK18	AVDD28_DAC	Y29	IDDIG
AG8	KP_COL6	A19	EWR#	AA29	USB_VBUS
AH8	KP_ROW6	B19	EA9	AB29	USB11_DP
AJ8	BPI_BUS2	C19	EA7	AC29	USB11_DM
A9	ED22	D19	RVREF	AD29	SRST2
B9	ED18	E19	/EDQS1	AF29	AVDD18_AUD
D9	ED21	J19	VSS	AG29	CF
E9	EDQS2	M19	VDDK_VSRAM	AH29	HSN
F9	VDD_EMI	N19	VSS	AJ29	HPRP

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K9	SDA_1	P19	VSS	AK29	COUT_AVSS12N
AB9	DVDD_NML2	R19	VSS	A30	CORNER
AC9	DVDD_NML4	T19	VSS	B30	NLD15
AF9	KP_COL0	U19	VSS	C30	NLD10
AJ9	BPI_BUS1	V19	VDDK	D30	NLD9
AK9	BPI_BUS0	AC19	3G_VBIAS	F30	NREB
A10	ED1	AG19	AUX_XP	G30	NLD12
B10	ED3	AH19	AUX_XM	J30	MSDC2_DAT1
E10	/EDQS2	AJ19	AUX_IN4	K30	MSDC1_DAT1
J10	VSS	AK19	AVDD25_VDAC	M30	MSDC0_DAT7
K10	SCL_1	A20	EBA0	N30	MSDC0_DAT6
N10	DVDD_LCD	B20	EA10	R30	JTRST_B
P10	DVDD_LCD	C20	EA13	T30	JTCK
AC10	KP_ROW1	D20	ED10	V30	PACTRL0
AF10	BPI_BUS3	E20	EDQS1	W30	SYSRST_B
AG10	BPI_BUS4	H20	AVSS25_MEMPLL	AA30	USB_VRT
AJ10	BPI_BUS5	J20	VSS	AB30	AVDD30_VSIM
AK10	BPI_BUS9	M20	VDDK_DVFS	AD30	SIO2
A11	DQM0	N20	VDDK_DVFS	AE30	AVDD30_VSIM2
B11	ED6	P20	VDDK_DVFS	AG30	CF_IN
C11	ED0	R20	VDDK_DVFS	AH30	AUDREFN
D11	ED7	T20	VDDK_DVFS	AJ30	AVSS12N_DAC
G11	VDD_EMI	U20	VDDK_DVFS	AK30	CORNER
K11	PWM4	V20	VDDK_DVFS		
N11	DVDD_LCD	AC20	AVSS25_MD		
P11	VDDK	AF20	DL_I_P		

2.1.3 Detailed Pin Description

Table 2-1: Acronym for pin type.

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Pin Name	Type	Description	Power Domain

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SYSTEM			
WATCHDOG_B	DO	Watchdog reset output	DVDD_NML2
SRCLKENAI	DIO	26MHz co-clock enable input	DVDD_NML5
SRCLKENA	DIO	26MHz co-clock enable output	DVDD_NML5
SYSRST_B	DI	System reset input	DVDD_NML5
LCD			
LPA0	DIO	Parallel display interface address output	DVDD_LCD
LPCE1B	DIO	Parallel display interface chip select 1 output	DVDD_LCD
LPTE	DIO	Parallel display interface tearing effect	DVDD_LCD
LWRB	DIO	Parallel display interface Write Strobe	DVDD_LCD
LPCE0B	DIO	Parallel display interface chip select 0 output	DVDD_LCD
LRDB	DIO	Parallel display interface Read Strobe	DVDD_LCD
LRSTB	DIO	Parallel display interface Reset Signal	DVDD_LCD
DPI			
DPIDE	DIO	Data enable signal of DPI	DVDD_LCD
DPICK	DIO	Clock pin of DPI	DVDD_LCD
DPIVSYNC	DIO	Vertical synchronization signal of DPI	DVDD_LCD
DPIHSYNC	DIO	Horizontal synchronization signal of DPI	DVDD_LCD
DPIR7	DIO	Data pin 7 of DPI R-channel / Data 23 for DBI parallel LCD interface	DVDD_LCD
DPIR6	DIO	Data pin 6 of DPI R-channel / Data 22 for DBI parallel LCD interface	DVDD_LCD
DPIR5	DIO	Data pin 5 of DPI R-channel / Data 21 for DBI parallel LCD interface	DVDD_LCD
DPIR4	DIO	Data pin 4 of DPI R-channel / Data 20 for DBI parallel LCD interface	DVDD_LCD
DPIR3	DIO	Data pin 3 of DPI R-channel / Data 19 for DBI parallel LCD interface	DVDD_LCD
DPIR2	DIO	Data pin 2 of DPI R-channel / Data 18 for DBI parallel LCD interface	DVDD_LCD
DPIR1	DIO	Data pin 1 of DPI R-channel / Data 17 for DBI parallel LCD interface	DVDD_LCD
DPIR0	DIO	Data pin 0 of DPI R-channel / Data 16 for DBI parallel LCD interface	DVDD_LCD
DPIG7	DIO	Data pin 7 of DPI G-channel / Data 15 for DBI parallel LCD interface	DVDD_LCD
DPIG6	DIO	Data pin 6 of DPI G-channel / Data 14 for DBI parallel LCD interface	DVDD_LCD
DPIG5	DIO	Data pin 5 of DPI G-channel / Data 13 for DBI parallel LCD interface	DVDD_LCD
DPIG4	DIO	Data pin 4 of DPI G-channel / Data 12 for DBI parallel LCD interface	DVDD_LCD
DPIG3	DIO	Data pin 3 of DPI G-channel / Data 11 for DBI parallel LCD interface	DVDD_LCD
DPIG2	DIO	Data pin 2 of DPI G-channel / Data 10 for DBI parallel LCD interface	DVDD_LCD
DPIG1	DIO	Data pin 1 of DPI G-channel / Data 9 for DBI parallel LCD interface	DVDD_LCD
DPIG0	DIO	Data pin 0 of DPI G-channel / Data 8 for DBI parallel LCD interface	DVDD_LCD
DPIB7	DIO	Data pin 7 of DPI B-channel / Data 7 for DBI parallel LCD interface	DVDD_LCD
DPIB6	DIO	Data pin 6 of DPI B-channel / Data 6 for DBI parallel LCD interface	DVDD_LCD
DPIB5	DIO	Data pin 5 of DPI B-channel / Data 5 for DBI parallel LCD interface	DVDD_LCD
DPIB4	DIO	Data pin 4 of DPI B-channel / Data 4 for DBI parallel LCD interface	DVDD_LCD
DPIB3	DIO	Data pin 3 of DPI B-channel / Data 3 for DBI parallel LCD interface	DVDD_LCD
DPIB2	DIO	Data pin 2 of DPI B-channel / Data 2 for DBI parallel LCD interface	DVDD_LCD
DPIB1	DIO	Data pin 1 of DPI B-channel / Data 1 for DBI parallel LCD interface	DVDD_LCD
DPIB0	DIO	Data pin 0 of DPI B-channel / Data 0 for DBI parallel LCD interface	DVDD_LCD
SLCD			

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LSCE0B	DIO	Serial display interface chip select 0 output	DVDD_LCD
LSDI	DIO	Serial display interface data input	DVDD_LCD
LSA0	DIO	Serial display interface address output	DVDD_LCD
LSCE1B	DIO	Serial display interface chip select 1 output	DVDD_LCD
LSCK	DIO	Serial display interface clock output	DVDD_LCD
LSDA	DIO	Serial display interface data	DVDD_LCD
I2S0			
I2S0_DAT	DIO	I2S0 data pin	DVDD_NML1
I2S0_WS	DIO	I2S0 word select	DVDD_NML1
I2S0_CK	DIO	I2S0 clock	DVDD_NML1
I2S1			
I2S1_CK	DIO	I2S1 data pin	DVDD_NML1
I2S1_WS	DIO	I2S1 word select	DVDD_NML1
I2S1_DAT	DIO	I2S1clock	DVDD_NML1
EINT			
EINT8	DIO	External interrupt 8	DVDD_NML1
EINT9	DIO	External interrupt 9	DVDD_NML1
EINT3	DIO	External interrupt 3	DVDD_NML2
EINT0	DIO	External interrupt 0	DVDD_NML2
EINT4	DIO	External interrupt 4	DVDD_NML2
EINT7	DIO	External interrupt 7	DVDD_NML2
EINT6	DIO	External interrupt 6	DVDD_NML2
EINT1	DIO	External interrupt 1	DVDD_NML2
EINT2	DIO	External interrupt 2	DVDD_NML2
EINT5	DIO	External interrupt 5	DVDD_NML2
DAI			
DAIPCMOUT	DIO	DAI data output	DVDD_NML1
DAICLK	DIO	DAI clock	DVDD_NML1
DAIPCMIN	DIO	DAI data input	DVDD_NML1
BTSYNC	DIO	BT sync signal	DVDD_NML1
DAIRSTB	DIO	DAI reset_	DVDD_NML1
PWM			
PWM2	DIO	PWM2	DVDD_NML2
PWM1	DIO	PWM1	DVDD_NML2
PWM3	DIO	PWM3	DVDD_NML2
PWM4	DIO	PWM4	DVDD_CAM
UART3			
UTXD3	DIO	UART3 TX	DVDD_NML2
URXD3	DIO	UART3 RX	DVDD_NML2
UART2			
UTXD2	DIO	UART2 TX	DVDD_NML2
URXD2	DIO	UART2 RX	DVDD_NML2
UCTS2	DIO	UART2 CTS	DVDD_NML2

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URTS2	DIO	UART2 RTS	DVDD_NML2
SPI			
SPI_CSN	DIO	SPI chip select	DVDD_NML3
SPI_MI	DIO	SPI data in	DVDD_NML3
SPI_MO	DIO	SPI data out	DVDD_NML3
SPI_CLK	DIO	SPI clock	DVDD_NML3
I2C0			
SCL_0	DIO	I2C0 clock	DVDD_NML3
SDA_0	DIO	I2C0 data	DVDD_NML3
MSDC3			
MSDC3_DAT2	DIO	MSDC3 data2 pin	DVDD_MC3
MSDC3_DAT1	DIO	MSDC3 data1 pin	DVDD_MC3
MSDC3_CMD	DIO	MSDC3 command pin	DVDD_MC3
MSDC3_CLK	DIO	MSDC3 clock output	DVDD_MC3
MSDC3_DAT3	DIO	MSDC3 data3 pin	DVDD_MC3
MSDC3_DAT0	DIO	MSDC3 data0 pin	DVDD_MC3
KP			
KP_COL7	DIO	Keypad column 7	DVDD_NML4
KP_COL6	DIO	Keypad column 6	DVDD_NML4
KP_COL5	DIO	Keypad column 5	DVDD_NML4
KP_COL4	DIO	Keypad column 4	DVDD_NML4
KP_COL3	DIO	Keypad column 3	DVDD_NML4
KP_COL2	DIO	Keypad column 2	DVDD_NML4
KP_COL1	DIO	Keypad column 1	DVDD_NML4
KP_COL0	DIO	Keypad column 0	DVDD_NML4
KP_ROW7	DIO	Keypad row 7	DVDD_NML4
KP_ROW6	DIO	Keypad row 6	DVDD_NML4
KP_ROW5	DIO	Keypad row 5	DVDD_NML4
KP_ROW4	DIO	Keypad row 4	DVDD_NML4
KP_ROW3	DIO	Keypad row 3	DVDD_NML4
KP_ROW2	DIO	Keypad row 2	DVDD_NML4
KP_ROW1	DIO	Keypad row 1	DVDD_NML4
KP_ROW0	DIO	Keypad row 0	DVDD_NML4
BPI			
BPI_BUS3	DIO	BPI BUS3	DVDD_BPI
TDD_AFC_SW	DIO	TDD_AFC_SW	DVDD_BPI
BPI_BUS1	DIO	BPI BUS1	DVDD_BPI
BPI_BUS4	DIO	BPI BUS4	DVDD_BPI
BPI_BUS0	DIO	BPI BUS0	DVDD_BPI
BPI_BUS5	DIO	BPI BUS5	DVDD_BPI
BPI_BUS2	DIO	BPI BUS2	DVDD_BPI
BPI_BUS8	DIO	BPI BUS8	DVDD_BPI
BPI_BUS9	DIO	BPI BUS9	DVDD_BPI

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BPI_BUS7	DIO	BPI BUS7	DVDD_BPI
BPI_BUS6	DIO	BPI BUS6	DVDD_BPI
TDD_TIMINGSYNC	DIO	TDD_TIMINGSYNC	DVDD_BPI
BPI_BUS10	DIO	BPI BUS10	DVDD_BPI
BPI_BUS14	DIO	BPI BUS14	DVDD_BPI
BPI_BUS13	DIO	BPI BUS13	DVDD_BPI
BPI_BUS11	DIO	BPI BUS11	DVDD_BPI
BPI_BUS12	DIO	BPI BUS12	DVDD_BPI
VM			
VM1	DIO	PA mode selection	DVDD_BPI
VM0	DIO	PA mode selection	DVDD_BPI
BSI			
BSI0_CS1	DIO	BSI0 CS1	DVDD_BSI
BSI1_DATA	DIO	BSI1 DATA	DVDD_BSI
BSI1_CS1	DIO	BSI1 CS1	DVDD_BSI
BSI1_CS0	DIO	BSI1 CS0	DVDD_BSI
BSI1_CLK	DIO	BSI1 CLK	DVDD_BSI
BSI0_DATA	DIO	BSI0 DATA	DVDD_BSI
BSI0_CS0	DIO	BSI0 CS0	DVDD_BSI
BSI0_CLK	DIO	BSI0 CLK	DVDD_BSI
PMIC			
SDA_2	DIO	I2C2 data	DVDD_NML5
PACTRL2	DIO	PMIC PA control 2	DVDD_NML5
PMUCTRL0	DIO	PMIC DVS control 0	DVDD_NML5
SYSRST_B	DIO	System reset input	DVDD_NML5
SCL_2	DIO	I2C2 clock	DVDD_NML5
PACTRL1	DIO	PMIC PA control 1	DVDD_NML5
PMUCTRL1	DIO	PMIC DVS control 1	DVDD_NML5
PACTRL0	DIO	PMIC PA control 0	DVDD_NML5
Coresight			
SWCLKTCK	DIO	Coresight debug interface : clock pin	DVDD_NML6
SWDIOTMS	DIO	Coresight debug interface : data pin	DVDD_NML6
JTAG			
JTCK	DIO	JTCK	DVDD_NML6
JTDO	DIO	JTDO	DVDD_NML6
JTRST_B	DIO	JTRST_B	DVDD_NML6
JTDI	DIO	JTDI	DVDD_NML6
JRTCK	DIO	JRTCK	DVDD_NML6
JTMS	DIO	JTMS	DVDD_NML6
UART4			
UTXD4	DIO	UART4 TX	DVDD_NML6
URXD4	DIO	UART4 RX	DVDD_NML6
UART1			

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URXD1	DIO	UART1 RX	DVDD_NML6
URTS1	DIO	UART1 RTS	DVDD_NML6
UCTS1	DIO	UART1 CTS	DVDD_NML6
UTXD1	DIO	UART1 TX	DVDD_NML6
MSDC0			
MSDC0_DAT6	DIO	MSDC0 data6 pin	DVDD_MC0
MSDC0_DAT7	DIO	MSDC0 data7 pin	DVDD_MC0
MSDC0_DAT5	DIO	MSDC0 data5 pin	DVDD_MC0
MSDC0_RSTB	DIO	MSDC0 reset output	DVDD_MC0
MSDC0_DAT4	DIO	MSDC0 data4 pin	DVDD_MC0
MSDC0_DAT2	DIO	MSDC0 data2 pin	DVDD_MC0
MSDC0_DAT3	DIO	MSDC0 data3 pin	DVDD_MC0
MSDC0_CMD	DIO	MSDC0 command pin	DVDD_MC0
MSDC0_CLK	DIO	MSDC0 clock output	DVDD_MC0
MSDC0_DAT1	DIO	MSDC0 data1 pin	DVDD_MC0
MSDC0_DAT0	DIO	MSDC0 data0 pin	DVDD_MC0
MSDC1_SDWPI	DIO	MSDC1 WP pin	DVDD_MC0
MSDC1			
MSDC1_DAT1	DIO	MSDC1 data1 pin	DVDD_MC1
MSDC1_DAT2	DIO	MSDC1 data2 pin	DVDD_MC1
MSDC1_DAT0	DIO	MSDC1 data0 pin	DVDD_MC1
MSDC1_DAT3	DIO	MSDC1 data3 pin	DVDD_MC1
MSDC1_CLK	DIO	MSDC1 clock output	DVDD_MC1
MSDC1_CMD	DIO	MSDC1 command pin	DVDD_MC1
MSDC1_INSI	DIO	MSDC1 card insertion	DVDD_NML6
MSDC2			
MSDC2_CLK	DIO	MSDC2 clock output	DVDD_MC2
MSDC2_DAT3	DIO	MSDC2 data3 pin	DVDD_MC2
MSDC2_CMD	DIO	MSDC2 command pin	DVDD_MC2
MSDC2_DAT2	DIO	MSDC2 data2 pin	DVDD_MC2
MSDC2_DAT0	DIO	MSDC2 data0 pin	DVDD_MC2
MSDC2_DAT1	DIO	MSDC2 data1 pin	DVDD_MC2
NFI			
NLD12	DIO	Parallel LCD/Nand-Flash Data 12	DVDD_NFI
NLD6	DIO	Parallel LCD/Nand-Flash Data 6	DVDD_NFI
NREB	DIO	Parallel NAND interface read strobe output	DVDD_NFI
NLD3	DIO	Parallel LCD/Nand-Flash Data 3	DVDD_NFI
NLD11	DIO	Parallel LCD/Nand-Flash Data 11	DVDD_NFI
NLD5	DIO	Parallel LCD/Nand-Flash Data 5	DVDD_NFI
NLD9	DIO	Parallel LCD/Nand-Flash Data 9	DVDD_NFI
NCEB1	DIO	Parallel NAND interface chip select 1 output	DVDD_NFI
NLD10	DIO	Parallel LCD/Nand-Flash Data 10	DVDD_NFI
NCEB0	DIO	Parallel NAND interface chip select 0 output	DVDD_NFI

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NLD4	DIO	Parallel LCD/Nand-Flash Data 4	DVDD_NFI
NWEB	DIO	Parallel NAND interface write strobe output	DVDD_NFI
NALE	DIO	Parallel NAND interface address latch enable output	DVDD_NFI
NLD15	DIO	Parallel LCD/Nand-Flash Data 15	DVDD_NFI
NLD14	DIO	Parallel LCD/Nand-Flash Data 14	DVDD_NFI
NLD2	DIO	Parallel LCD/Nand-Flash Data 2	DVDD_NFI
NRNB	DIO	Parallel NAND interface chip ready input	DVDD_NFI
NLD1	DIO	Parallel LCD/Nand-Flash Data 1	DVDD_NFI
NLD8	DIO	Parallel LCD/Nand-Flash Data 8	DVDD_NFI
NLD7	DIO	Parallel LCD/Nand-Flash Data 7	DVDD_NFI
NCLE	DIO	Parallel NAND interface command latch enable output	DVDD_NFI
NLD13	DIO	Parallel LCD/Nand-Flash Data 13	DVDD_NFI
NLD0	DIO	Parallel LCD/Nand-Flash Data 0	DVDD_NFI
EFUSE			
FSOURCE	DIO	E-FUSE Blowing Power Control	AVDD25_MEMPLL
EMI			
/ECS0	DIO	DRAM chip select 0 #	DVDD_EMI
/ECS1	DIO	DRAM chip select 1 #	DVDD_EMI
/EDCLK	DIO	DRAM clock output #	DVDD_EMI
/EDQS0	DIO	DRAM DQS 0 #	DVDD_EMI
/EDQS1	DIO	DRAM DQS 1 #	DVDD_EMI
/EDQS2	DIO	DRAM DQS 2 #	DVDD_EMI
/EDQS3	DIO	DRAM DQS 3 #	DVDD_EMI
DDR3RSTB	DIO	DDR3 reset output #	DVDD_EMI
DQM0	DIO	DRAM DQM 0	DVDD_EMI
DQM1	DIO	DRAM DQM 1	DVDD_EMI
DQM2	DIO	DRAM DQM 2	DVDD_EMI
DQM3	DIO	DRAM DQM 3	DVDD_EMI
EA0	DIO	DRAM address output 0	DVDD_EMI
EA1	DIO	DRAM address output 1	DVDD_EMI
EA10	DIO	DRAM address output 10	DVDD_EMI
EA11	DIO	DRAM address output 11	DVDD_EMI
EA12	DIO	DRAM address output 12	DVDD_EMI
EA13	DIO	DRAM address output 13	DVDD_EMI
EA2	DIO	DRAM address output 2	DVDD_EMI
EA3	DIO	DRAM address output 3	DVDD_EMI
EA4	DIO	DRAM address output 4	DVDD_EMI
EA5	DIO	DRAM address output 5	DVDD_EMI
EA6	DIO	DRAM address output 6	DVDD_EMI
EA7	DIO	DRAM address output 7	DVDD_EMI
EA8	DIO	DRAM address output 8	DVDD_EMI
EA9	DIO	DRAM address output 9	DVDD_EMI
EBA0	DIO	DRAM bank address output 0	DVDD_EMI

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EBA1	DIO	DRAM bank address output 1	DVDD_EMI
ECAS#	DIO	DRAM command output CAS#	DVDD_EMI
ECKE0	DIO	DRAM command output CKE	DVDD_EMI
ED0	DIO	DRAM data pin 0	DVDD_EMI
ED1	DIO	DRAM data pin 1	DVDD_EMI
ED10	DIO	DRAM data pin 10	DVDD_EMI
ED11	DIO	DRAM data pin 11	DVDD_EMI
ED12	DIO	DRAM data pin 12	DVDD_EMI
ED13	DIO	DRAM data pin 13	DVDD_EMI
ED14	DIO	DRAM data pin 14	DVDD_EMI
ED15	DIO	DRAM data pin 15	DVDD_EMI
ED16	DIO	DRAM data pin 16	DVDD_EMI
ED17	DIO	DRAM data pin 17	DVDD_EMI
ED18	DIO	DRAM data pin 18	DVDD_EMI
ED19	DIO	DRAM data pin 19	DVDD_EMI
ED2	DIO	DRAM data pin 2	DVDD_EMI
ED20	DIO	DRAM data pin 20	DVDD_EMI
ED21	DIO	DRAM data pin 21	DVDD_EMI
ED22	DIO	DRAM data pin 22	DVDD_EMI
ED23	DIO	DRAM data pin 23	DVDD_EMI
ED24	DIO	DRAM data pin 24	DVDD_EMI
ED25	DIO	DRAM data pin 25	DVDD_EMI
ED26	DIO	DRAM data pin 26	DVDD_EMI
ED27	DIO	DRAM data pin 27	DVDD_EMI
ED28	DIO	DRAM data pin 28	DVDD_EMI
ED29	DIO	DRAM data pin 29	DVDD_EMI
ED3	DIO	DRAM data pin 3	DVDD_EMI
ED30	DIO	DRAM data pin 30	DVDD_EMI
ED31	DIO	DRAM data pin 31	DVDD_EMI
ED4	DIO	DRAM data pin 4	DVDD_EMI
ED5	DIO	DRAM data pin 5	DVDD_EMI
ED6	DIO	DRAM data pin 6	DVDD_EMI
ED7	DIO	DRAM data pin 7	DVDD_EMI
ED8	DIO	DRAM data pin 8	DVDD_EMI
ED9	DIO	DRAM data pin 9	DVDD_EMI
EDCLK	DIO	DRAM clock output	DVDD_EMI
EDQS0	DIO	DRAM DQS 0	DVDD_EMI
EDQS1	DIO	DRAM DQS 1	DVDD_EMI
EDQS2	DIO	DRAM DQS 2	DVDD_EMI
EDQS3	DIO	DRAM DQS 3	DVDD_EMI
ERAS#	DIO	DRAM command output RAS#	DVDD_EMI
EWR#	DIO	DRAM command output WR#	DVDD_EMI
RVREF	DIO	Voltage reference input	DVDD_EMI

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CAM			
CMDAT2	DIO	Pixel data [2] from sensor	DVDD_CAM
CMMCLK	DIO	Master clock to sensor	DVDD_CAM
CMDAT7	DIO	Pixel data [7] from sensor	DVDD_CAM
CMDAT0	DIO	Pixel data [0] from sensor	DVDD_CAM
CMDAT4	DIO	Pixel data [4] from sensor	DVDD_CAM
CMDAT6	DIO	Pixel data [6] from sensor	DVDD_CAM
CMDAT3	DIO	Pixel data [3] from sensor	DVDD_CAM
CMDAT8	DIO	Pixel data [8] from sensor	DVDD_CAM
CMDAT9	DIO	Pixel data [9] from sensor	DVDD_CAM
CMRST	DIO	Reset control to sensor	DVDD_CAM
CMDAT5	DIO	Pixel data [5] from sensor	DVDD_CAM
CMVSYNC	DIO	VREF from sensor	DVDD_CAM
CMPCLK	DIO	Pixel clock from sensor	DVDD_CAM
CMHSYNC	DIO	HREF from sensor	DVDD_CAM
CMPDN	DIO	Power down to sensor	DVDD_CAM
CMDAT1	DIO	Pixel data [1] from sensor	DVDD_CAM
CMFLASH	DIO	Camera flash control signal	DVDD_CAM
I2C1			
SCL_1	DIO	I2C1 clock	DVDD_CAM
SDA_1	DIO	I2C1 data	DVDD_CAM
RTC			
RTC_XIN	AIO	RTC crystal in	AVDD28_RTC
RTC_XOUT	AIO	RTC crystal out	AVDD28_RTC
BBWAKEUP	AIO	Wakeup signal to external PMIC	AVDD28_RTC
TESTMODE	AIO	Test mode	AVDD28_RTC
32K_OUT	AIO	32K clock output	AVDD28_RTC
ABB			
APC	AIO	Automatic power control	AVDD28_DAC
AFC	AIO	Automatic frequency control	AVDD28_DAC
3G_VBIAS	AIO	3G PA analog control	AVDD28_DAC
VDAC_OUT	AIO	Video DAC output	AVDD25_MD
AUX_YP	AIO	Aux ADC channel for touch screen TP_Y+	AVDD25_MD
AUX_YM	AIO	Aux ADC channel for touch screen TP_Y-	AVDD25_MD
AUX_XP	AIO	Aux ADC channel for touch screen TP_X+	AVDD25_MD
AUX_XM	AIO	Aux ADC channel for touch screen TP_X-	AVDD25_MD
AUX_IN4	AIO	Aux ADC external channel 4	AVDD25_MD
AUX_IN3	AIO	Aux ADC external channel 3	AVDD25_MD
AUX_IN2	AIO	Aux ADC external channel 2	AVDD25_MD
AUX_IN1	AIO	Aux ADC external channel 1	AVDD25_MD
AUX_IN0	AIO	Aux ADC external channel 0	AVDD25_MD
DL_Q_P	AIO	UMTS downlink for UMTSRX_QP	AVDD25_VDAC
DL_Q_N	AIO	UMTS downlink for UMTSRX_QN	AVDD25_VDAC

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DL_I_N	AIO	UMTS downlink for UMTSRX_IN	AVDD25_VDAC
DL_I_P	AIO	UMTS downlink for UMTSRX_IP	AVDD25_VDAC
UL_Q_N	AIO	UMTS uplink for GSM_UMTSTX_QN	AVDD25_VDAC
UL_Q_P	AIO	UMTS uplink for GSM_UMTSTX_QP	AVDD25_VDAC
UL_I_P	AIO	UMTS uplink for GSM_UMTSTX_IP	AVDD25_VDAC
UL_I_N	AIO	UMTS uplink for GSM_UMTSTX_IN	AVDD25_VDAC
REFN	AI	Reference voltage for LDO, tie to GND	AVDD25_VDAC
REFP	AI	Reference voltage for LDO, tie to GND with 1uF capacitor	AVDD25_VDAC
VMIC	AIO	MIC bias for main & reference MIC	AVDD25_VDAC
AU_VIN0_P	AIO	Audio 0 in P for microphone	AVDD25_VDAC
AU_VIN0_N	AIO	Audio 0 in N for microphone	AVDD25_VDAC
AU_VIN1_P	AIO	Audio 1 in P for microphone	AVDD25_VDAC
AU_VIN1_N	AIO	Audio 1 in N for microphone	AVDD25_VDAC
AU_VIN2_P	AIO	Audio 2 in P for microphone	AVDD25_VDAC
AU_VIN2_N	AIO	Audio 2 in N for microphone	AVDD25_VDAC
EARBIAS	AIO	MIC bias for earphone MIC	AVDD25_VDAC
ACCDET	AIO	Plug-in/out detection signal for headset	AVDD25_VDAC
ANASWCTRL	AIO	Analog switch control	AVDD25_VDAC
HSP	AIO	AUDIO_OUT_P for handset receiver	AVDD25_VBUF
COUT_AVSS12N	AIO	-1.2V charge-pump output	AVDD18_AUD
HSN	AIO	AUDIO_OUT_N for handset receiver	AVDD25_VBUF
CF	AIO	Charge-pump flying cap. negative input	AVDD18_AUD
FMINL	AIO	Audio interface for FM_LINE_IN_L	AVDD18_AUD
AUDREFN	AIO	Earphone receiver signal for AUDIO_JACK_GND	AVDD18_AUD
FMINR	AIO	Audio interface for FM_LINE_IN_R	AVDD18_AUD
CF_IN	AIO	Charge-pump flying cap. positive input	AVDD18_AUD
HPLP	AIO	Earphone receiver signal for AUDIO_JACK_L	AVDD18_AUD
HPRP	AIO	Earphone receiver signal for AUDIO_JACK_R	AVDD18_AUD
SIM			
SIO2	AIO	SIM2 data	AVDD30_VSIM2
SRST2	AIO	SIM2 reset	AVDD30_VSIM2
SCLK2	AIO	SIM2 clock	AVDD30_VSIM2
SIO	AIO	SIM1 data	AVDD30_VSIM
SRST	AIO	SIM1 reset	AVDD30_VSIM
SCLK	AIO	SIM1 clock	AVDD30_VSIM
USB20			
CHD_DM	AIO	BC1.1 Charger DM	AVDD33_USB
CHD_DP	AIO	BC1.1 Charger DP	AVDD33_USB
IDDIG	DIO	USB OTG ID pin	DVDD_NML5
USB_VBUS	AI	Power for connected device +3.3V	AVDD33_USB
USB_DM	AIO	USB D- differential data line	AVDD33_USB
USB_DP	AIO	USB D+ differential data line	AVDD33_USB
USB_VRT	AO	USB output for bias current; connect with 5.11K 1% Ohm to GND	AVDD33_USB

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USB11			
USB11_DM	AIO	USB D- differential data line	AVDD33_USB11
USB11_DP	AIO	USB D+ differential data line	AVDD33_USB11
MEMPLL			
MEMPLL_TXP	AIO	MEMPLL different output P for debug	AVDD25_MEMPLL
MEMPLL_TXN	AIO	MEMPLL different output N for debug	AVDD25_MEMPLL
MIPI			
RDN0	AIO	CSI2 data lane 0	DVDD18_MIPIRX
RDP0	AIO	CSI2 data lane 0	DVDD18_MIPIRX
RDN1	AIO	CSI2 data lane 1	DVDD18_MIPIRX
RDP1	AIO	CSI2 data lane 1	DVDD18_MIPIRX
RCN	AIO	CSI2 clock lane	DVDD18_MIPIRX
RCP	AIO	CSI2 clock lane	DVDD18_MIPIRX
TDP0	AIO	DSI data lane 0	DVDD18_MIPITX
TDN0	AIO	DSI data lane 0	DVDD18_MIPITX
TDP1	AIO	DSI data lane 1	DVDD18_MIPITX
TDN1	AIO	DSI data lane 1	DVDD18_MIPITX
TCP	AIO	DSI clock lane	DVDD18_MIPITX
TCN	AIO	DSI clock lane	DVDD18_MIPITX
Analog Power			
AVDD18_MIPI	P	Analog power input 1.8V for MIPI	-
AVDD18_MD	P	Analog power input 1.8V for ABB	-
AVDD18_AUD	P	Analog power input 1.8V for Audio	-
AVDD25_VBUF	P	Analog power input 2.5V for Voice Buffer	-
AVDD25_PLL	P	Analog power input 2.5V for PLL	-
AVDD25_MD	P	Analog power input 2.5V for ABB	-
AVDD25_MEMPLL	P	Analog power input 2.5V for MEMPLL	-
AVDD28_RTC	P	Analog power output 2.8V for real-time clock	-
AVDD28_DAC	P	Analog power input 2.8V for DAC	-
AVDD25_VDAC	P	Analog power input 2.5V for VDAC	-
AVDD30_VSIM	P	Analog power input 3V for VSIM	-
AVDD30_VSIM2	P	Analog power input 3V for VSIM2	-
AVDD33_USB	P	Analog power output 3.3V for USB	-
AVDD33_USB11	P	Analog power output 3.3V for USB11	-
Digital Power			
DVDD18_MIPITX	P	Digital power input 1.8V for MIPITX	-
DVDD18_MIPIRX	P	Digital power input 1.8V for MIPIRX	-
DVDD_NFI	P	Digital power input for NFI	-
DVDD_BPI	P	Digital power input for BPI	-
DVDD_BSI	P	Digital power input for BSI	-
DVDD_CAM	P	Digital power input for camera	-
DVDD_EMI	P	Digital power input for EMI	-
DVDD_LCD	P	Digital power input for LCD	-

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DVDD_MC0	P	Digital power input for MSDC0	-
DVDD_MC1	P	Digital power input for MSDC1	-
DVDD_MC2	P	Digital power input for MSDC2	-
DVDD_MC3	P	Digital power input for MSDC3	-
DVDD_NML1	P	Digital power input1	-
DVDD_NML2	P	Digital power input2	-
DVDD_NML3	P	Digital power input3	-
DVDD_NML4	P	Digital power input4	-
DVDD_NML5	P	Digital power input5	-
DVDD_NML6	P	Digital power input6	-
VDDK	P	Digital power input for core	-
VDDK_DVFS	P	Digital power input for processor	-
VDDK_VSRAM	P	Digital power input for processor memory	-
Analog Ground			
AVSS12N_DAC	G		-
AVSS18_AUD	G		-
AVSS18_MD	G		-
AVSS18_MIPI	G		-
AVSS25_MD	G		-
AVSS25_MEMPLL	G		-
AVSS25_PLL	G		-
AVSS25_VDAC	G		-
AVSS28_RTC	G		-
AVSS30_VSIM	G		-
AVSS33_USB	G		-
AVSS33_USB11	G		-
Digital Ground			
DVSS18_MIPIRX	G		-
DVSS18_MIPITX	G		-
VSS	G		-

2.2 Electrical characteristics

2.2.1 Absolute maximum ratings

Table 2-2: Absolute maximum ratings for power supply.

Symbol or Pin Name	Description	Min.	Max.	Unit
AVDD18_MIPI	Analog power input 1.8V for MIPI	1.7	1.9	V
AVDD18_MD	Analog power input 1.8V for ABB	1.7	1.9	V
AVDD18_AUD	Analog power input 1.8V for Audio	1.7	1.9	V
AVDD25_VBUF	Analog power input 2,5V for Voice Buffer	2.375	2.625	V
AVDD25_PLL	Analog power input 2,5V for PLL	2.375	2.625	V
AVDD25_MD	Analog power input 2,5V for ABB	2.375	2.625	V

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Symbol or Pin Name	Description	Min.	Max.	Unit
AVDD25_MEMPLL	Analog power input 2,5V for MEMPLL	2.375	2.625	V
AVDD28_RTC	Analog power output 2.8V for real-time clock	2.66	2.94	V
AVDD28_DAC	Analog power input 2,8V for DAC	2.66	2.94	V
AVDD25_VDAC	Analog power input 2,5V for VDAC	2.375	2.625	V
AVDD30_VSIM	Analog power input 3V for VSIM	1.7	3.15	V
AVDD30_VSIM2	Analog power input 3V for VSIM2	1.7	3.15	V
AVDD33_USB	Analog power output 3.3V for USB	3.315	3.465	V
AVDD33_USB11	Analog power output 3.3V for USB11	3.315	3.465	V
DVDD18_MIPITX	Digital power input 1.8V for MIPITX	1.62	1.98	V
DVDD18_MIPIRX	Digital power input 1.8V for MIPIRX	1.62	1.98	V
DVDD_NFI	Digital power input for NFI	1.62	1.98	V
DVDD_BPI	Digital power input for BPI	2.6	3.0	V
DVDD_BSI	Digital power input for BSI	1.62	1.98	V
DVDD_CAM	Digital power input for camera	1.62	3.0	V
DVDD_EMI	Digital power input for EMI	1.08	1.98	V
DVDD_LCD	Digital power input for LCD	1.62	3.0	V
DVDD_MC0	Digital power input for MSDC0	1.62	3.63	V
DVDD_MC1	Digital power input for MSDC1	1.62	3.63	V
DVDD_MC2	Digital power input for MSDC2	1.62	3.63	V
DVDD_MC3	Digital power input for MSDC3	1.62	3.63	V
DVDD_NML1	Digital power input1	1.62	3.0	V
DVDD_NML2	Digital power input2	1.62	3.0	V
DVDD_NML3	Digital power input3	1.62	3.0	V
DVDD_NML4	Digital power input4	1.62	3.0	V
DVDD_NML5	Digital power input5	1.62	3.0	V
DVDD_NML6	Digital power input6	1.62	3.0	V
VDDK	Digital power input for core	1.0	1.21	V
VDDK_DVFS	Digital power input for processor	1.08	1.32	V
VDDK_VSRAM	Digital power input for processor memory	1.08	1.32	V

Warning: Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only.

2.2.2 Recommended operating conditions

Table 2-3: Recommended operating conditions for power supply.

Symbol or Pin Name	Description	Min.	Typ.	Max.	Unit
AVDD18_MIPI	Analog power input 1.8V for MIPI	1.7	1.8	1.9	V
AVDD18_MD	Analog power input 1.8V for ABB	1.7	1.8	1.9	V
AVDD18_AUD	Analog power input 1.8V for Audio	1.7	1.8	1.9	V
AVDD25_VBUF	Analog power input 2,5V for Voice Buffer	2.38	2.5	2.62	V
AVDD25_PLL	Analog power input 2,5V for PLL	2.38	2.5	2.62	V
AVDD25_MD	Analog power input 2,5V for ABB	2.38	2.5	2.62	V
AVDD25_MEMPLL	Analog power input 2,5V for MEMPLL	2.38	2.5	2.62	V
AVDD28_RTC	Analog power output 2.8V for real-time clock	2.66	2.8	2.94	V
AVDD28_DAC	Analog power input 2,8V for DAC	2.66	2.8	2.96	V
AVDD25_VDAC	Analog power input 2,5V for VDAC	2.38	2.5	2.62	V
AVDD30_VSIM	Analog power input 3V for VSIM	2.86	3.0	3.14	V
AVDD30_VSIM2	Analog power input 3V for VSIM2	2.86	3.0	3.14	V
AVDD33_USB	Analog power output 3.3V for USB	3.16	3.3	3.46	V

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Symbol or Pin Name	Description	Min.	Typ.	Max.	Unit
AVDD33_USB11	Analog power output 3.3V for USB11	3.16	3.3	3.46	V
DVDD18_MIPITX	Digital power input 1.8V for MIPITX	1.7	1.8	1.9	V
DVDD18_MIPIRX	Digital power input 1.8V for MIPIRX	1.7	1.8	1.9	V
DVDD_NFI	Digital power input for NFI	1.7	1.8	1.9	V
DVDD_BPI	Digital power input for BPI	2.66	2.8	2.96	V
DVDD_BSI	Digital power input for BSI	1.7	1.8	1.9	V
DVDD_CAM	Digital power input for camera	1.7	1.8	1.9	V
DVDD_EMI	Digital power input for EMI	1.7	1.8	1.9	V
DVDD_LCD	Digital power input for LCD	1.62	1.8	1.98	V
DVDD_MC0	Digital power input for MSDC0	2.98	3.3	3.46	V
DVDD_MC1	Digital power input for MSDC1	2.98	3.3	3.46	V
DVDD_MC2	Digital power input for MSDC2	2.98	3.3	3.46	V
DVDD_MC3	Digital power input for MSDC3	2.98	3.3	3.46	V
DVDD_NML1	Digital power input1	1.7	1.8	1.9	V
DVDD_NML2	Digital power input2	1.7	1.8	1.9	V
DVDD_NML3	Digital power input3	1.7	1.8	1.9	V
DVDD_NML4	Digital power input4	1.7	1.8	1.9	V
DVDD_NML5	Digital power input5	1.7	1.8	1.9	V
DVDD_NML6	Digital power input6	1.7	1.8	1.9	V
VDDK	Digital power input for core	1.034	1.1	1.21	V
VDDK_DVFS	Digital power input for processor	1.25	1.25	1.3125	V
VDDK_VSRAM	Digital power input for processor memory	1.25	1.25	1.3125	V

2.2.3 Storage condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After bag opened, devices subjected to infrared reflow, vapor-phase reflow, or equivalent processing must be:
   A. Mounted within 168 hours at factory conditions of ≤ 30°C/60% RH, or
   B. Stored at ≤ 20% RH.
3. Devices require baking, before mounting, if:
   A. 192 hours at 40°C +5°C/-0°C and < 5% RH for low temperature device containers, or
   B. 24 hours at 125°C +5°C/-0°C for high temperature device containers.

2.2.4 AC electrical characteristics and timing diagram

2.2.4.1 External Memory Interface for LPDDR

External memory interface, shown in Figure 2-1, Figure 2-2 and Figure 2-3, is used to connect LPDDR device for MT6575. It includes the pins ED_CLK, ED_CLK_B, ECKE, ECS#, EWR#, ERAS#, ECAS#, EDQS[3:0], EA[13:0] and ED[31:0]. Table 2-4 summarizes the symbol definition and the related timing specification

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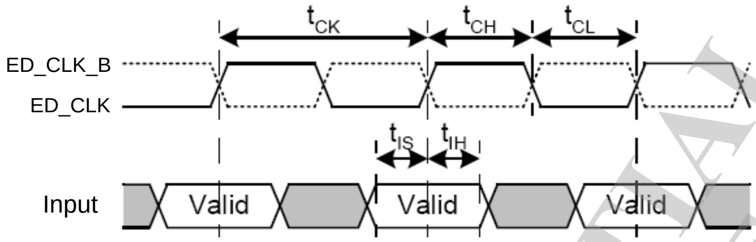
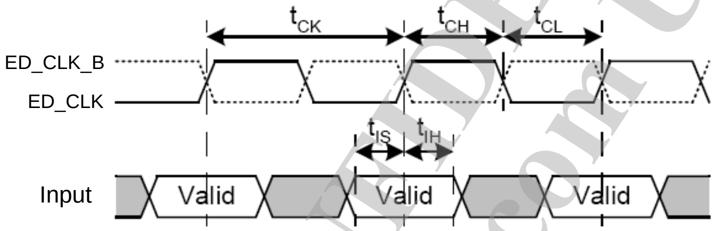


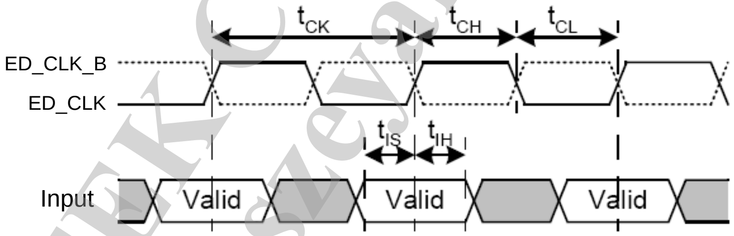
Input = EA0~EA13, ECKE, ECS#, EWR#, ERAS#, and ECAS#

Figure 2-1: Basic Timing Parameter for LPDDR Commands.



Input = EA0~EA13, ECKE, ECS#, EWR#, ERAS#, and ECAS#

Figure 2-2: Basic Timing Parameter for LPDDR Write.



Input = EA0~EA13, ECKE, ECS#, EWR#, ERAS#, and ECAS#

Figure 2-3: Basic LPDDR Read Timing Parameter.

Table 2-4: The LPDDR AC timing parameter table of external memory interface.

Symbol	Description	Min.	Typ.	Max.	Unit
tAC[1]	DQ output access time from CK/CK’	2.0		5.0	ns
tDQSCK[1]	DQS output access time from CK/CK’	2.0		5.0	ns
tCK	Clock cycle time	5.0			ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tHP	Clock half period	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.58			ns
tDH	DQ & DM input hold time	0.58			ns
tIS	Address & control input setup time	1.1			ns

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Symbol	Description	Min.	Typ.	Max.	Unit
tIH	Address & control input hold time	1.1			ns
tLZ[1]	DQ & DQS low-impedance time from CK/CK’	1.0			ns
tHZ[1]	DQ & DQS high-impedance time from CK/CK’			5.0	ns
tDQSQ[1]	DQS-DQ skew			0.4	ns
tQH[1]	DQ/DQS output hold time from DQS	tHP-tQHS			
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tMRD[2]	MODE register set command period	2			tCK
tRPRE[1]	Read preamble	0.9		1.1	tCK
tRPST[1]	Read postamble	0.4		0.6	tCK
tRAS[2]	ACTIVE to PRECHARGE command period	8			tCK
tRC[2]	ACTIVE to ACTIVE command period	11			tCK
tRFC[2]	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	28			tCK
tRCD[2]	ACTIVE to READ or WRITE delay	3			tCK
tRP[2]	PRECHARGE command period	3			tCK
tRRD[2]	ACTIVE bank A to ACTIVE bank B delay	2			tCK
tWR[2]	WRITE recovery time	3			tCK
tWTR[2]	Internal write to READ command time	2			tCK
tXSR[2]	SELF REFRESH exit to next valid command	40			tCK
tXP[2]	EXIT power down to next valid command delay	2			tCK
tCKE[2]	CKE min. pulse width (high & low pulse width)	2			tCK
tREF[2]	Refresh Period			64	ms

2.2.4.2 External Memory Interface for LPDDR2

External memory interface, shown in Figure 2-4, Figure 2-5 and Figure 2-6, is used to connect LPDDR2 device for MT6575. It includes the pins ED_CLK, ED_CLK_B, ECKE, ECS#, EBA[2:0], EDQS[3:0], EDQS#[3:0], EA[9:0] and ED[31:0]. Table 2-5 summarizes the symbol definition and the related timing specification

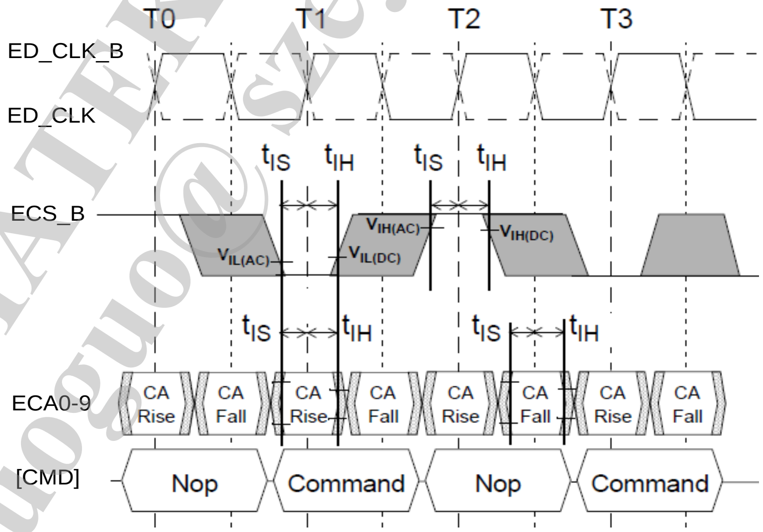

Figure 2-4: Basic Timing Parameter for LPDDR2 Commands.

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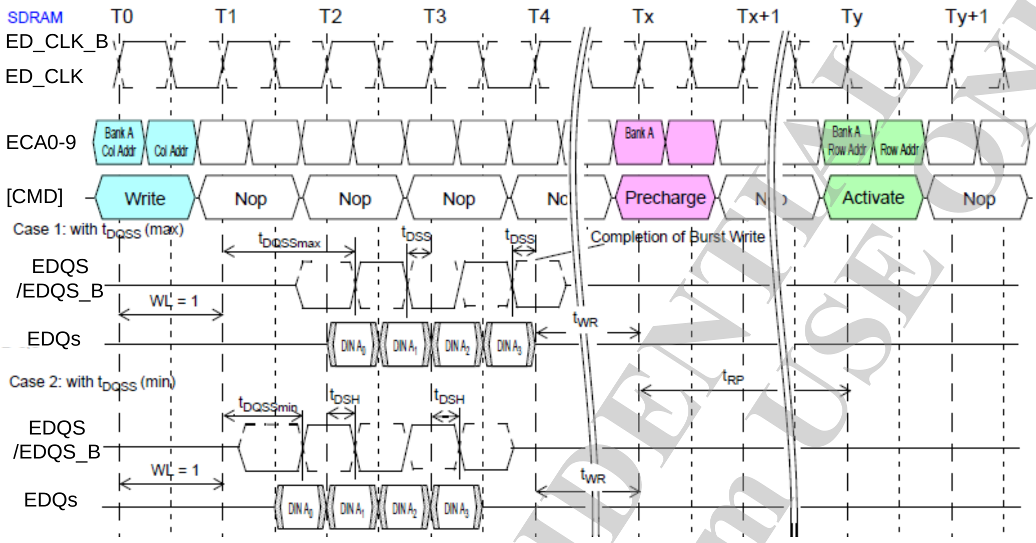

Figure 2-5: Basic Timing Parameter for LPDDR2 Write.

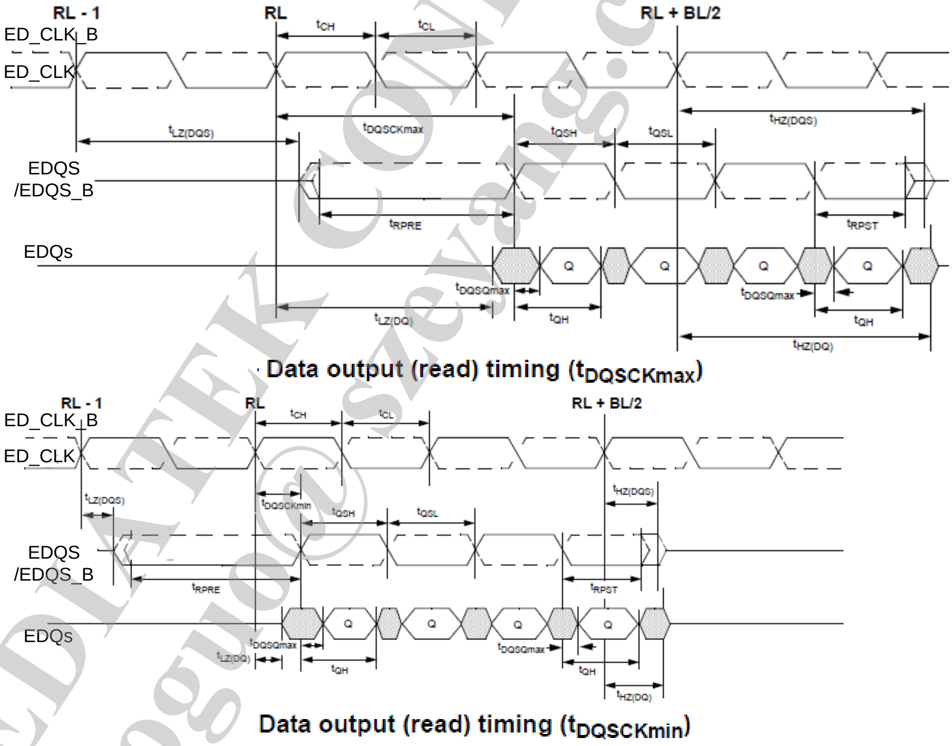

Figure 2-6: Basic LPDDR2 Read Timing Parameter.

Table 2-5: The LPDDR2 AC timing parameter table of external memory interface.

Symbol	Description	Min.	Typ.	Max.	Unit

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Symbol	Description	Min.	Typ.	Max.	Unit
tCK[3]	Clock Cycle Time	3.75		8	ns
tDQSCK1	DQS output access time from CK/CK'	2.5		5.5	ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tHP	Clock half period	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.43			ns
tDH	DQ & DM input hold time	0.43			ns
tDQSS	Write command to 1st DQS latching transition	0.75		1.25	tCK
tDSS	DQS falling edge to CK setup time	0.2			tCK
tDSH	DQS falling edge hold time from CK	0.2			tCK
tIS	Address & control input setup time	0.46			ns
tIH	Address & control input hold time	0.46			ns
tLZ(DQS)1	DQS low-impedance time from CK/CK'	tDQSCK (MIN) - 300			ns
tHZ(DQS)1	DQS high-impedance time from CK/CK'			tDQSCK (MAX) - 100	ns
tLZ(DQ)1	DQ low-impedance time from CK/CK'	tDQSCK(MIN) - (1.4 × tQHS(MAX))			ns
tHZ(DQ)1	DQ high-impedance time from CK/CK'			tDQSCK(MAX) + (1.4 × tDQSQ(MAX))	ns
tDQSQ1	DQS-DQ skew			0.34	ns
tQHP	Data half period	MIN (tQSH, tQSL)			tCK
tQHS	Data hold skew factor			0.4	ns
tQH1	DQ/DQS output hold time from DQS	tQHP - tQHS			ns
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tQSH	DQS output high pulse width	tCH - 0.05			tCK
tQSL	DQS output low pulse width	tCL - 0.05			tCK
tMRW[4]	MODE register Write command period	5			tCK
tMRR[5]	MODE register Read command period	2			tCK
tRPRE1	Read preamble	0.9		1.1	tCK
tRPST1	Read postamble	tCL - 0.05			tCK
tRAS2	ACTIVE to PRECHARGE command period	3			tCK
tRC2	ACTIVE to ACTIVE command period	6			tCK
tRFC2	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	56			tCK
tRCD2	ACTIVE to READ or WRITE delay	3			tCK
tRP2	PRECHARGE command period	3			tCK
tRRD2	ACTIVE bank A to ACTIVE bank B delay	2			tCK
tWR2	WRITE recovery time	3			tCK
tWTR2	Internal write to READ command time	2			tCK
tXSR2	SELF REFRESH exit to next valid command	40			tCK
tXP2	EXIT power down to next valid command delay	2			tCK
tCKE2	CKE min. pulse width (high & low pulse width)	2			tCK
tREF2	Refresh Period			32	ms

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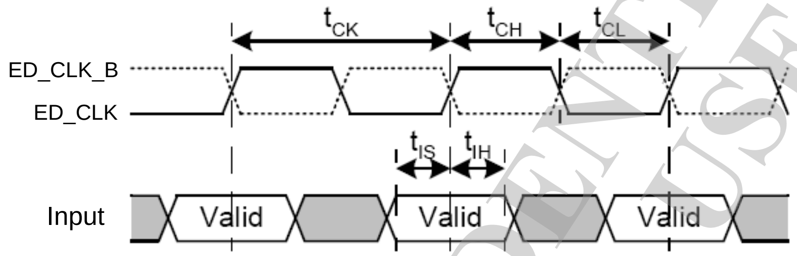
2.2.4.3 External Memory Interface for DDR3

External memory interface, shown in, is used to connect DDR3 device for MT6575. It includes the pins ED_CLK, ED_CLK_B, RESET_B, ECKE, ECS#, EWR#, ERAS#, ECAS#, EDQS[3:0], EDQS#[3:0], EA[13:0] and ED[31:0]. Table 2-6 summarizes the symbol definition and the related timing specification



Input = EA0~EA13, ECKE, ECS#, EWR#, ERAS#, and ECAS#

Figure 2-7: Basic Timing Parameter for DDR3 Commands.

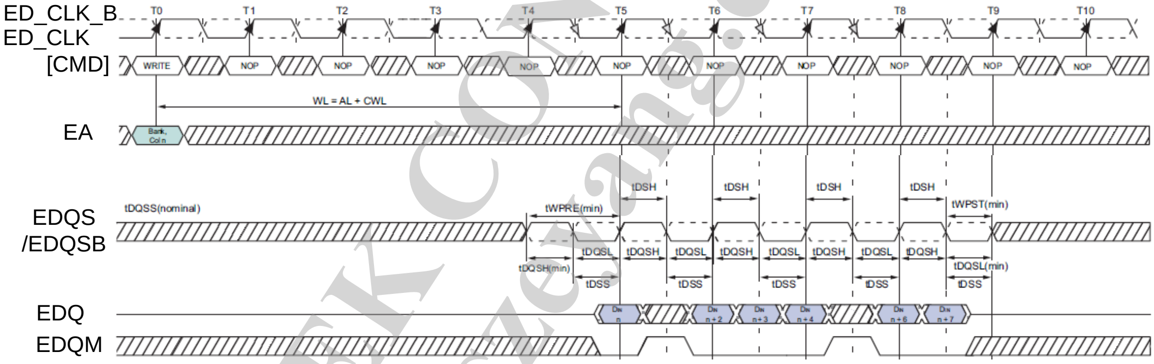


Figure 2-8: Basic Timing Parameter for DDR3 Write.

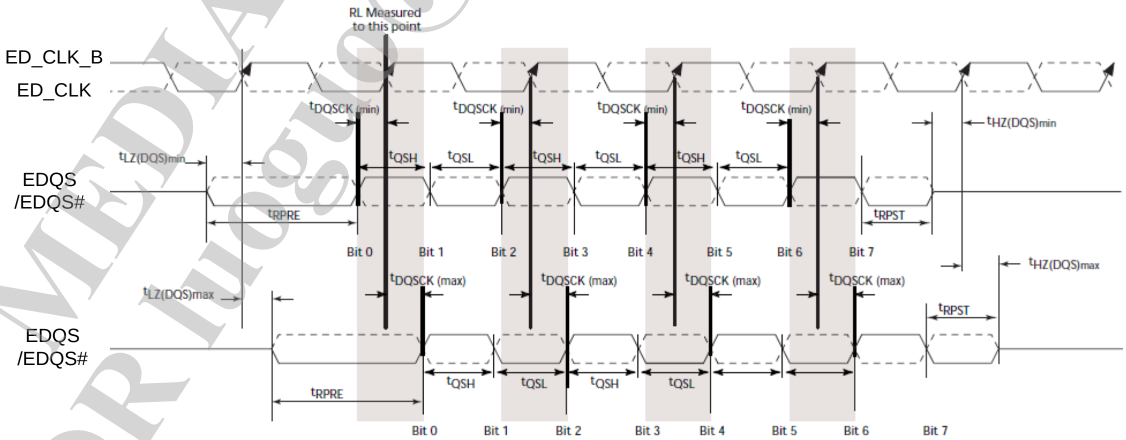


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Figure 2-9: Basic Timing Parameter for DDR3 Read.

Table 2-6: The DDR3 AC timing parameter table of external memory interface.

Symbol	Description	Min.	Typ.	Max.	Unit
tDQSCK1	DQS output access time from CK/CK’	-0.4		0.4	ns
tCK	Clock cycle time	2.5		3.75	ns
tCH	Clock high level width	0.47		0.53	tCK
tCL	Clock low level width	0.47		0.53	tCK
tDS	DQ & DM input setup time	0.125			ns
tDH	DQ & DM input hold time	0.15			ns
tIS	Address & control input setup time	0.35			ns
tIH	Address & control input hold time	0.275			ns
tLZ1	DQ & DQS low-impedance time from CK/CK’	-0.8			ns
tHZ1	DQ & DQS high-impedance time from CK/CK’			0.4	ns
tDQSQ1	DQS-DQ skew			0.2	ns
tQH1	DQ/DQS output hold time from DQS	0.38			tCK
tDQSH	DQS input high-level width	0.45		0.55	tCK
tDQSL	DQS input low-level width	0.45		0.55	tCK
tMRD[6]	MODE register set command period	4			tCK
tRPRE1	Read preamble	0.9			tCK
tRPST1	Read postamble	0.3			tCK
tRAS2	ACTIVE to PRECHARGE command period	10			tCK
tRC2	ACTIVE to ACTIVE command period	14			tCK
tRFC2	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	94			tCK
tRCD2	ACTIVE to READ or WRITE delay	4			tCK
tRP2	PRECHARGE command period	4			tCK
tRRD2	ACTIVE bank A to ACTIVE bank B delay	4			tCK
tWR2	WRITE recovery time	4			tCK
tWTR2	Internal write to READ command time	4			tCK
tXSDLL2	Exit Self Refresh to command requiring a locked DLL	512			tCK
tXPDLL2	Exit power down with DLL frozen to commands requiring a locked DLL	10			tCK
tXP2	EXIT power down with DLL to next valid command delay	3			tCK
tCKE2	CKE min. pulse width (high & low pulse width)	3			tCK
tREFI	Average periodic refresh interval	3.9			us

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2.3 System Configuration

2.3.1 Mode Selection

Table 2-7: Mode Selection of Chip.

Pin Name	Description
KP_COL0	0: Trigger USB download without battery 1: NA
KP_ROW0	0: Trigger USB download without battery 1: NA

2.3.2 Constant Tied Pins

Table 2-8: Constant Tied Pins of Chip.

Pin Name	Description
TESTMODE	Test mode (tie to GND)
FSOURCE	EFUSE burning (tie to GND)

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2.4 Power-on Sequence

The power-on/off sequence which is controlled by “Control” and “Reset Generator” is shown as follows,

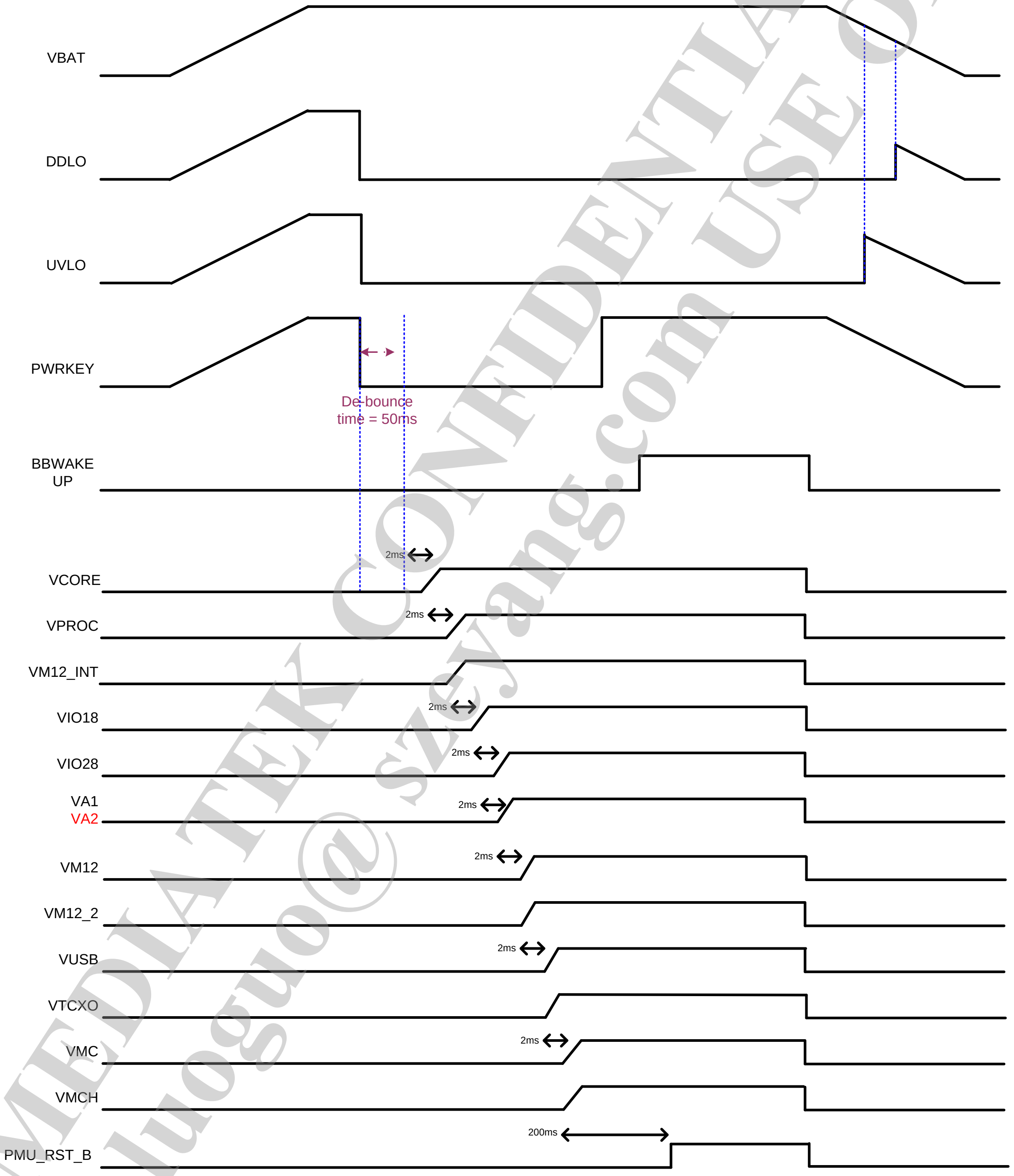

Figure 2-10: Power on/off Control Sequence

Note that the above figure only shows one power-on/off condition. External PMIC MT6329 for application processor MT6575 handles the powering ON and OFF of the handset. The following three different ways can switch-on the handset (When VBAT>=3.2V):

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Pulling PWRKEY low (User push PWRKEY)
Pulling BBWAKEUP high (Baseband BB_WakeUp)
Valid charger plug-in

Pulling PWRKEY low is a normal way to turn on the handset. That will turn on regulators as long as the PWRKEY is kept low. MT6329 output reset signal PMU_RST_B to MT6575 SYSRST_B input. After SYSRST_B de-asserted, the microprocessor then starts and pulls BBWAKEUP high. After that PWRKEY can be released. Pulling BBWAKEUP high will also turn on the handset. This is the case when the alarm in the RTC expires.

Besides, applying a valid external supply on CHRIN will also turn on the handset. However, If the battery is in UV state (VBAT<3.2V), the handset can't be turned-on in any way.

The UVLO function in the MT6329 prevents system startup when initial voltage of the main battery is below the 3.2V threshold. When the battery voltage is greater than 3.2V, the UVLO comparator switches and the threshold is reduced to 2.9V. This allows the handset to start smoothly unless the battery decays to 2.9V and below.

Once the MT6329 enters UVLO state, it draws very low quiescent current. The VRTC LDO is still active until the DDLO disables it.

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2.5 Analog Baseband

2.5.1 BBRX

2.5.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

1. Analog input multiplexer: For each channel, a 4-input multiplexer that supports offset and gain calibration is included.
2. A/D converter: 2 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

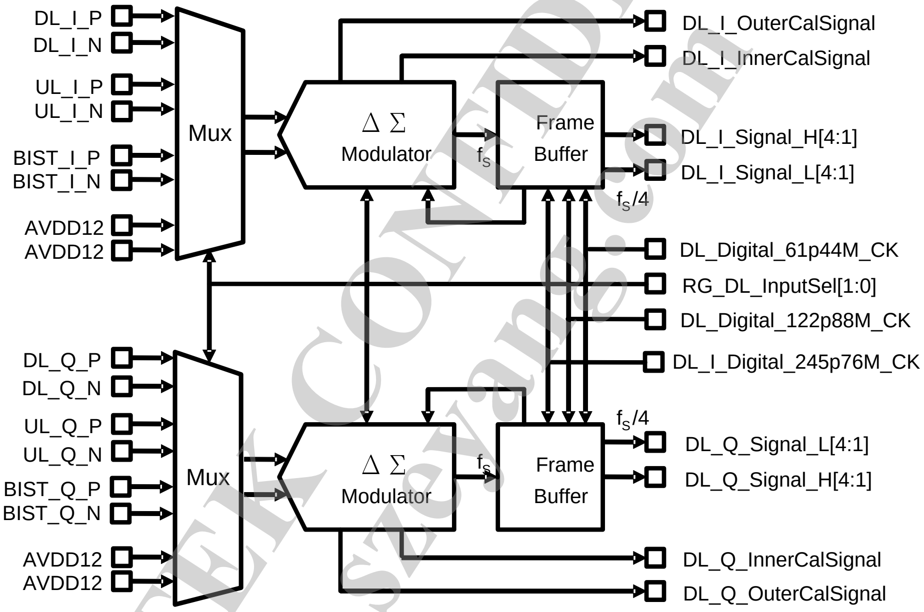

Figure 2-11: Block diagram of BBRX-ADC.

2.5.1.2 Functional Descriptions

See the table below for the function specifications of the base-band downlink receiver.

Table 2-9: Baseband downlink specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			4	V
ICM	Common mode input current magnitude			1	uA
VCM	Common mode input voltage	1.08	1.2	1.32	V
FC	Input clock frequency - Clock rate (WCDMA) - Clock rate (GSM)		 245.76 208		 MHz MHz
	Input clock duty cycle	49.5	50	50.5	%
	Input clock period jitter, WCDMA & TD-SCDMA configurations			0.14	% (rms)
	Input clock period jitter, GSM configurations			0.61	% (rms)
RIN	Differential input resistance	20	32.5	45	kΩ

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Symbol	Parameter	Min.	Typ.	Max.	Unit
FS	Output sampling rate		61.44/26		MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise - WCDMA configuration: 4Vpp(2.8 MHz) sinewave, 100 Hz ~ 1.92 MHz band - TD-CDMA configuration 4Vpp(1.6 MHz) sinewave, 100 Hz ~ 640 KHz band - GSM configuration: 4Vpp(200 KHz) sinewave, 217 Hz ~ 135 KHz band		75.4 79.3 85.5	78.4 83.5 90.9	dB dB dB
IM3	IM3 (with below inputs) - 10.08 MHz & 20.4 MHz (564mVpp) - 3.5 MHz & 5.9 MHz (710mVpp)			-61 -63	dBc dBc
IM2	IM2 (with the inputs as below) - 4.88 MHz & 5.12 MHz (448mVpp) - 14.88 MHz & 15.12 MHz (448mVpp)			-59 -59	dBc dBc
AVDD18	Digital power supply	1.7	1.8	1.9	V
AVDD25	Analog power supply	2.4	2.5	2.6	V
T	Operating temperature	-20		80	°C
	Current consumption (per channel) - Power-up (AVDD25) - Power-up (AVDD18) - Power-down(AVDD12@80C) - Power-down(AVDD12@125C)			1 1 1 3	mA mA uA uA

2.5.2 BBTX

2.5.2.1 Block Descriptions

The transmitter (Tx) performs baseband I/Q channels up-link digital-to-analog conversion. Each channel includes:

1. 11-bit D/A converter: Converts digital 8PSK/WCDMA modulated signals to analog domain. The input to the DAC is sampled at 61.44/26 MHz/ (3G/2G) rate with the 11-bit resolution.

2. Smoothing filter: The low-pass filter performs smoothing function for DAC output signals with a 9/1.8MHz (3G/2G) 2^{nd}-order Butterworth frequency response.

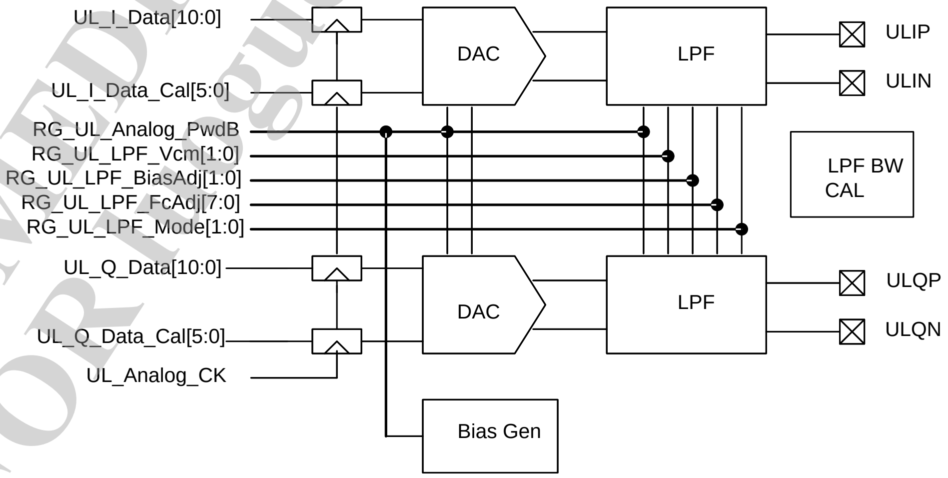

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Figure 2-12: Block diagram of BBTX-DAC.

2.5.2.2 Functional Descriptions

See the table below for the function specifications of the base-band uplink transmitter.

Table 2-10: Baseband uplink transmitter specifications.

Symbol	Parameter	Min	Typ.	Max	Unit
N	Resolution		11		Bit
FS	Sampling rate (3G/2G)		61.44/26		MSPS
SINAD	Signal to noise ratio (in-band) - 3G mode - 2G mode		70 80		dB dB
THD	- 3G mode - 2G mode		-50 -53		dB dB
	Output swing (full Swing)	0.9	1.0	1.1	Vppd
VOCM	Output CM voltage	1.15	1.2	1.25	V
	Output capacitance (single-ended)			20	PF
	Output resistance (differential)		1.5		KΩ
DNL	Differential nonlinearity	-0.5		+0.5	LSB
INL	Integral nonlinearity	-1.0		+1.0	LSB
OE	Offset error (after calibration)		+/- 1		LSB
FSE	Full swing error (Max.)		14		mV
FCUT	Filter -3dB cutoff frequency (calibrated) - 3G mode - 2G mode		8 1.8		MHz MHz
	I/Q gain mismatch		+/- 0.1		dB
	EVM (WCDMA modulation)		0.25	0.4	%
	ACLR1 (WCDMA modulation 5 MHz offset)		-65	-60	dB
	ACLR2 (WCDMA modulation 10 MHz offset)		-70	-65	dB
	Filter attenuation (3G mode) at - 7.5 ~ 12.5M - 12.5 ~ 40M - > 40 MHz		-140 -145 -160	-135 -140 -155	dBc/Hz dBc/Hz dBc/Hz
DVDD	Digital power supply	1.2	1.25	1.3	V
AVDD	Analog power supply	2.4	2.5	2.6	V
T	Operating temperature	-20		80	°C
	Current consumption - Power-up - Power-down		5.9 10		mA uA

2.5.3 APC-DAC

2.5.3.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at APC pin.

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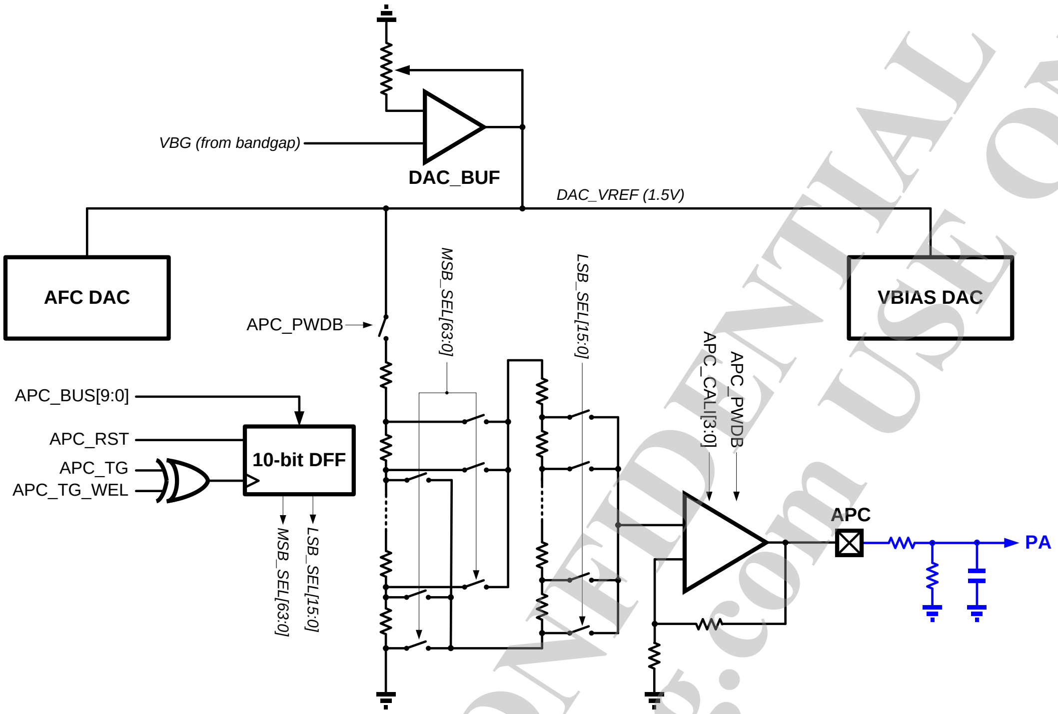

Figure 2-13: Block diagram of APC-DAC.

2.5.3.2 Functional Descriptions

See the table below for the function specifications of the APC-DAC.

Table 2-11: APC-DAC specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate			1.0833	MS/s
SNDR	Signal-to-noise-and-distortion ratio (10 kHz sine wave with 1.0V swing)		50		dB
T_S	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		200	220	pF
DNL	Differential nonlinearity (code 20 ~ 970)		±0.5		LSB
INL	Integral nonlinearity (code 20 ~ 970)		±1.0		LSB
DVDD	Digital power supply	1.1	1.2	1.3	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	–40		85	°C
I_{ON}	Current consumption (power on state)		200		uA
I_{OFF}	Current consumption (power down state)			1	uA

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2.5.4 AFC-DAC

2.5.4.1 Block Descriptions

See the figure below. AFC-DAC is designed to produce a single-ended output signal at AFC pin.

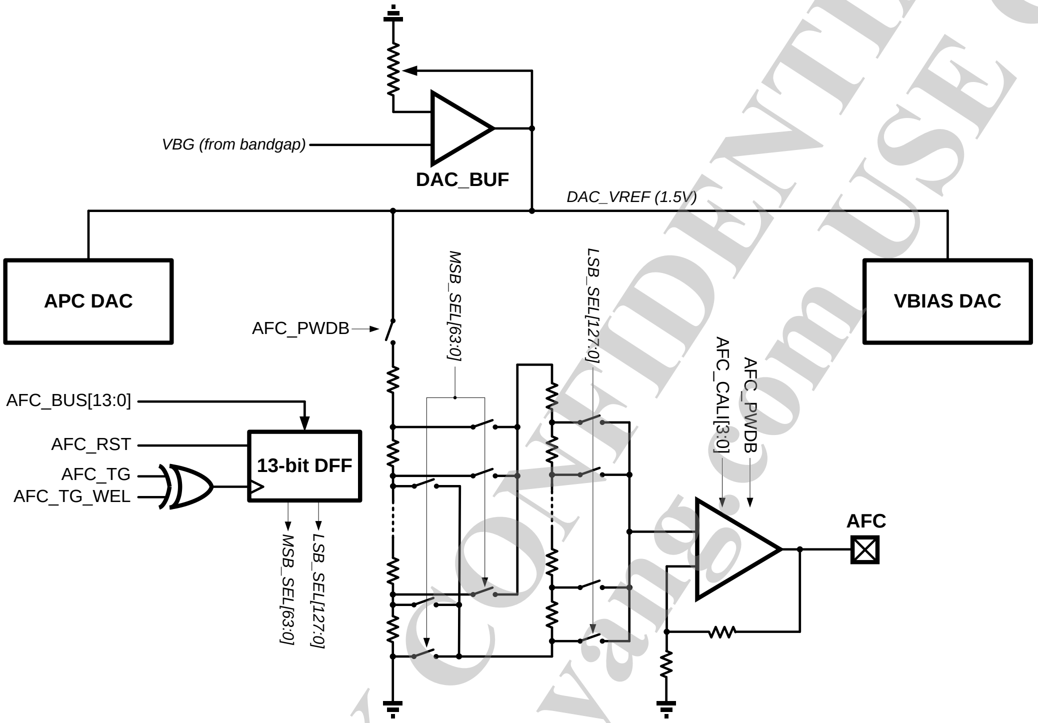

Figure 2-14: Block diagram of AFC-DAC.

2.5.4.2 Functional Descriptions

The functional specifications of the AFC-DAC are listed in the following table.

Table 2-12: AFC-DAC specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		13		Bit
F_S	Clock rate			1.0833	MS/s
T_S	Settling time (99% full-swing settling)			1	ms
C_L	Output loading capacitance			100	nF
DNL	Differential nonlinearity (0.35 ~ 2.45V)		±1.0		LSB
INL	Integral nonlinearity (0.35 ~ 2.45V)		±4.0		LSB
DVDD	Digital power supply	1.1	1.2	1.3	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	–40		85	°C
I_{ON}	Current consumption (power on state)		300		uA
I_{OFF}	Current consumption (power down state)			1	uA

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2.5.5 TVDAC

2.5.5.1 Block Descriptions

The 10-bit video DAC transforms the digital composite video signal (NTSC/PAL) to analog signal. See the tables in the following sections for the analog pin assignment and function specifications.

2.5.5.2 Functional Descriptions

See the table below for the function specifications of TVDAC.

Table 2-13: TVDAC specifications.

Symbol	Parameter	Min	Typical	Max	Unit
N	Resolution		10		Bit
FS	Sampling rate		27		MSPS
	Output current		26.67	35	mA
	Output loading resistance		37.5		Ω
DNL	Differential nonlinearity		+/- 1		LSB
INL	Integral nonlinearity		+/- 2		LSB
DVDD	Digital power supply	0.99	1.1	1.21	V
AVDD	Analog power supply	2.375	2.5	625	V
T	Operating temperature	-20		80	℃
	Current consumption Power-up Power-down		 37 	 1	 mA uA

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2.5.6 VBIAS-DAC

2.5.6.1 Block Descriptions

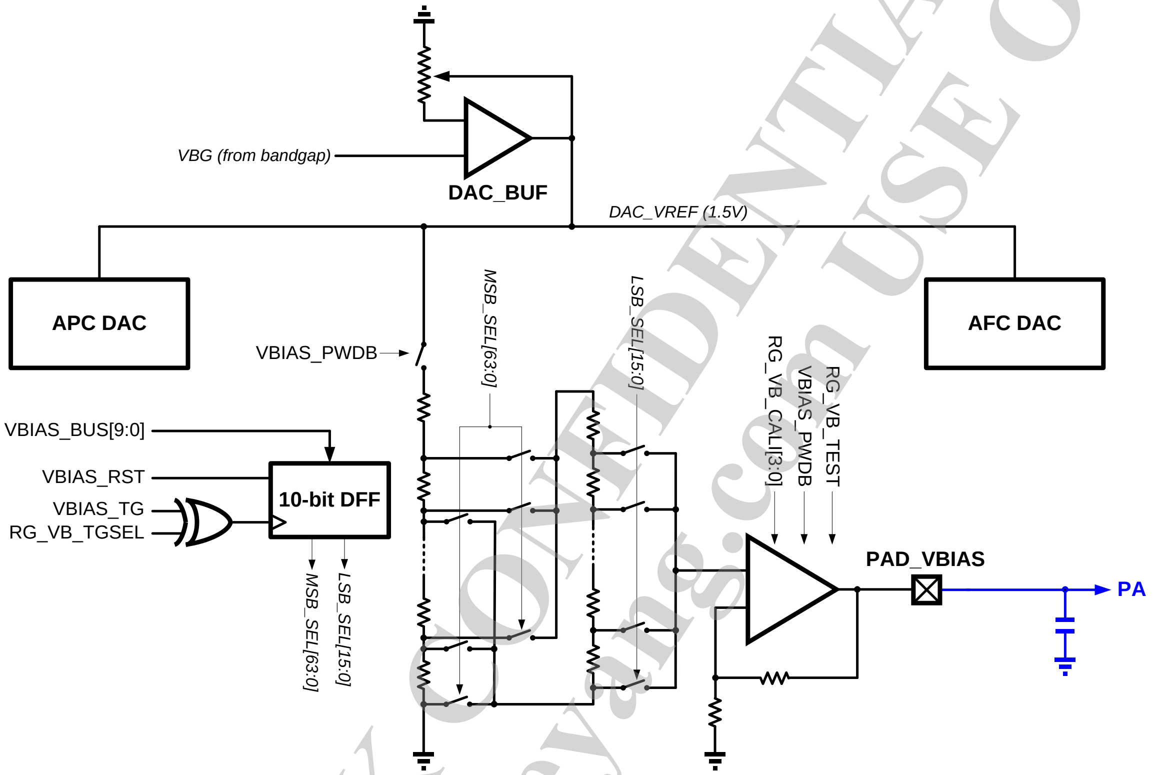

Figure 2-15: Block diagram of VBIAS-DAC.

2.5.6.2 Functional Descriptions

The functional specifications of the VBIAS-DAC are listed in the following table.

Table 2-14: VBIAS-DAC specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate			1.0833	MS/s
SNDR	Signal-to-noise-and-distortion ratio (10KHz sine wave with 1.0V swing)		50		dB
T_S	Settling time (99% full-swing settling)			3	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		1000		pF
DNL	Differential nonlinearity (code 20 ~ 970)		±0.5		LSB
INL	Integral nonlinearity (code 20 ~ 970)		±1.0		LSB
DVDD	Digital power supply	1.1	1.2	1.3	V
AVDD	Analog power supply	2.6	2.8	3.0	V

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Symbol	Parameter	Min.	Typ.	Max.	Unit
T	Operating temperature	–40		85	°C
I_{ON}	Current consumption (power on state)		200		uA
I_{OFF}	Current consumption (power down state)			1	uA

2.5.7 AUXADC

2.5.7.1 Block Descriptions

Auxiliary ADC measures ADC and is the resistive touch panel controller. The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measuring and some for external voltage measuring. Real-world messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

The touch screen controller drives the external touch panel via Pads XP, XM, YP and YM, and AUXADC as a voltage meter, obtains the X/Y-position of the touched point on the external touch screen. The touch screen interface contains 3 main blocks: touch screen pads control logic, ADC interface logic and interrupt generation logic. The touch screen interface supports 2 conversion modes: separate X/Y position conversion mode and auto (sequential) X/Y position conversion mode. See Table 2-15 for brief descriptions of AUXADC input channels.

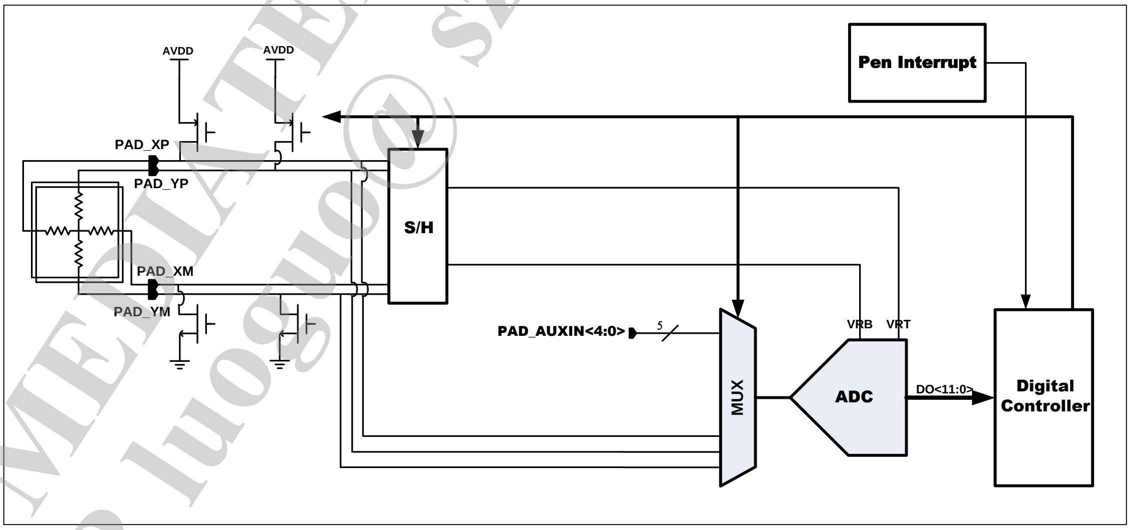

Figure 2-16: Block diagram of AUXADC.

Table 2-15: Definitions of AUXADC channels.

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AUXADC channel ID	Description
Channel 0	External use (AUX_IN0)
Channel 1	External use (AUX_IN1)
Channel 2	External use (AUX_IN2)
Channel 3	External use (AUX_IN3)
Channel 4	External use (AUX_IN4)
Channel 5	NA
Channel 6	NA
Channel 7	NA
Channel 8	NA
Channel 9	NA
Channel 10	NA
Channel 11	NA
Channel 12	XM (touch panel)
Channel 13	XP (Touch Panel)
Channel 14	YP (Touch Panel)
Channel 15	YM (Touch Panel)

2.5.7.2 Functional Descriptions

See the table below for the function specifications of auxiliary ADC.

Table 2-16: AUXADC specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		4		MHz
FS	Sampling rate @ N-Bit		4/(N+4)		MSPS
	Input swing	0		AVDD	V
CIN	Input capacitance Unselected channel Selected channel			50 6.4	fF pF
RIN	Input resistance Unselected channel	400			MΩ
	Clock latency		N+4		1/FC
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+1.0/-1.0		LSB
OE	Offset error		+/- 5		mV
FSE	Full swing error		+/- 5		mV
SINAD	Signal to noise and distortion ratio (10 kHz full swing input & 1.0833 MHz clock rate)	62	68		dB
DVDD	Digital power supply	1.0	1.1	1.2	V
AVDD	Analog power supply	2.4	2.5	2.6	V
T	Operating temperature	-20		80	°C
	Current consumption Power-up Power-down		250 1		uA uA
Ztp	Supported touch panel impedance	200		2K	Ω

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2.5.8 Audio Mixed-Signal Blocks

2.5.8.1 Block Descriptions

Audio mixed-signal blocks (AMB) integrate complete voice uplink/downlink and audio playback functions. As shown in the figure below, it includes 3 parts. The first consists of stereo audio DAC and audio amplifier for audio playback. The second part is the voice downlink path, including voice-band DAC (right channel audio DAC) and voice amplifier, which produces voice signal to earphone or other auxiliary output devices. Amplifiers in the two blocks are equipped with multiplexers to accept signals from internal audio/voice or external radio sources. The last part is the voice uplink path, which is the interface between the microphone (or other auxiliary input devices) input and DSP. A set of bias voltage is provided for the external electric microphone.

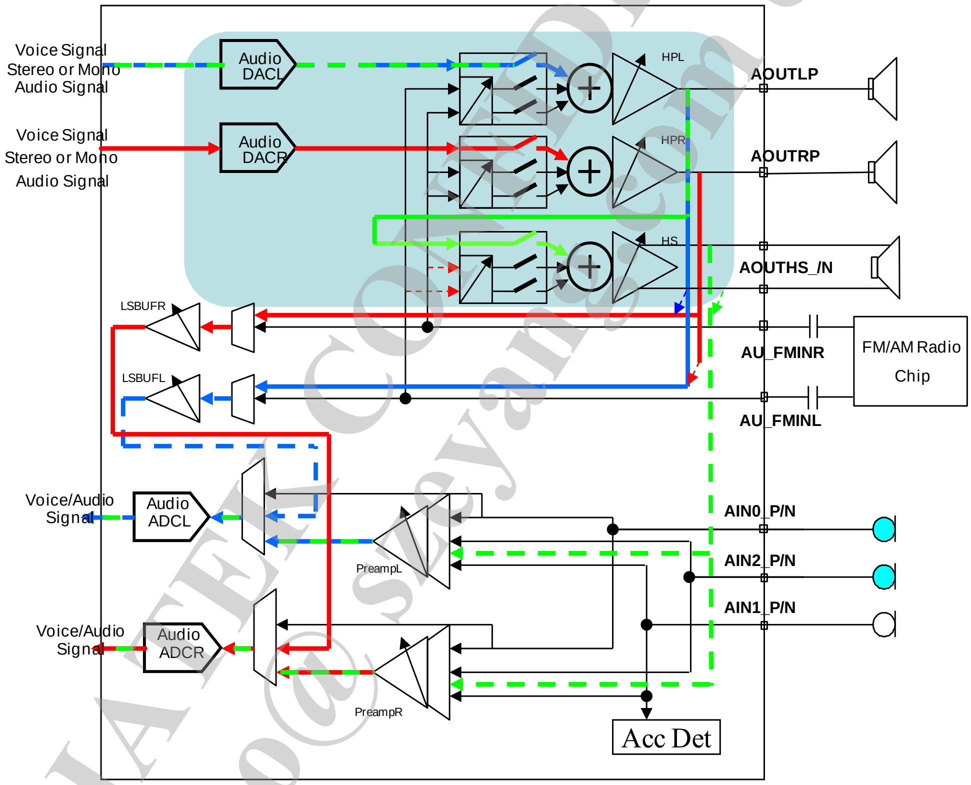

Figure 2-17: Block diagram of audio mixed-signal blocks.

2.5.8.2 Functional Descriptions

See the table below for the function specifications of voice-band uplink/downlink blocks.

Table 2-17: Analog voice specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T	Operating temperature	-20		80	°C
VMIC	Microphone biasing voltage		1.9		V

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Symbol	Parameter	Min.	Typ.	Max.	Unit
IMIC	Current draw from microphone bias		2		mA
Uplink path					
Analog MIC path					
IDC	Current consumption for single channel		1.5		mA
SINAD	Signal to noise and distortion ratio Input level: -40 dbm0 Input level: 0 dbm0	 29	 69		 dB dB
RIN	Input impedance (differential)	13	20	27	KΩ
ICN	Idle channel noise			-67	dBm0
XT	Crosstalk level			-66	dBm0
Digital MIC path					
DCLK	DMIC clock frequency		1.625 / 3.25		MHz
DTY	DMIC clock duty cycle	40		60	%
DCRT	DMIC clock rise time		10		ns
DCFT	DMIC clock fall time		10		ns
ICDD	Input capacitance for DMIC data			45	pF
Downlink path					
AVDD18	1.8V analog power supply	1.7	1.8	1.9	V
IDC	Quiescent current consumption		4.5		mA
SINAD	Signal to noise and distortion ratio Input level: -40 dBm0 Input level: 0 dBm0	 29	 69		 dB dB
RLOAD	Output resistor load	27			Ω
CLOAD	Output capacitor load		200	500	pF
ICN	Idle channel noise of transmit path			-67	dBm0

Table 2-18: Analog audio specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T	Operating temperature	-20		80	°C
AVDD18	1.8V analog power supply	1.7	1.8	1.9	V
IDC	Quiescent current consumption		6		mA
BW	Signal bandwidth	20		20,000	Hz
VOUT	Full-scale output signal level		0.5		Vrms
RLOAD	Output resistor load	16	32		Ω
CLOAD	Output capacitor load			200	pF
SNR	Signal to noise ratio		88		dB
DR	Dynamic range		88		dB
THD	Total harmonic distortion		-80	-70	dBc
XT	Channel separation (crosstalk)		80		dB

2.5.9 Clock Squarer

2.5.9.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make MT6575 digital circuits function well. Clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle. It provides also a pull-down function when the circuit is powered-down.

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2.5.9.2 Functional Descriptions

See the table below for the function specifications of clock squarer.

Table 2-19: Clock squarer specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Fout	Output clock frequency	13	26		MHz
Vin	Input signal amplitude	350	500	1000	mVpp
DcycIN	Input signal duty cycle		50		%
DcycOUT	Output signal duty cycle	DcycIN-5		DcycIN+5	%
TR	Rise time on Pin CLKSQOUT			5	ns/pF
TF	Fall time on Pin CLKSQOUT			5	ns/pF
DVDD	Digital power supply	1.0	1.1	1.2	V
AVDD	Analog power supply1 Analog power supply2	2.4 1.7	2.5 1.8	2.6 1.9	V
T	Operating temperature	-20		80	℃
	Current consumption		100		uA

2.5.10 Phase Lock Loop

2.5.10.1 Block Descriptions

There are total 8 PLLs and 1 DDS in PLL macro, providing several clocks for CPU, BUS, Modem, Analog modem, & Audio. ARMPLL & MAINPLL providing around 1GHz clock for ARM Cortex-A9. To support synchronous & asynchronous mode, ARMPLL & MAINPLL are enabled accordingly. ISPPLL is the clock source of image sense processing, which ranges 104~208MHz for supporting various image sensor. MDPLL is the main clock source of modem, providing a fixed 1040MHz for further clock division. USBPLL provides 48MHz to USB, and 4-phase 624MHz to TVDDS. TVDDS is a fractional frequency divider which generates 27/54/148.5MHz for TV/HDMI purpose. 3GPLL is a fractional PLL which multiply clock 26MHz to 983.04MHz, generating 245.76MHz to analog downlink ADC and other frequency to HSPA. AUDPLL is a 32k-based PLL which generating 208MHz for audio processing, and a low noise 26MHz for analog audio part. MEMPLL supports 195/260/390/520MHz for various DDR memory clocking.

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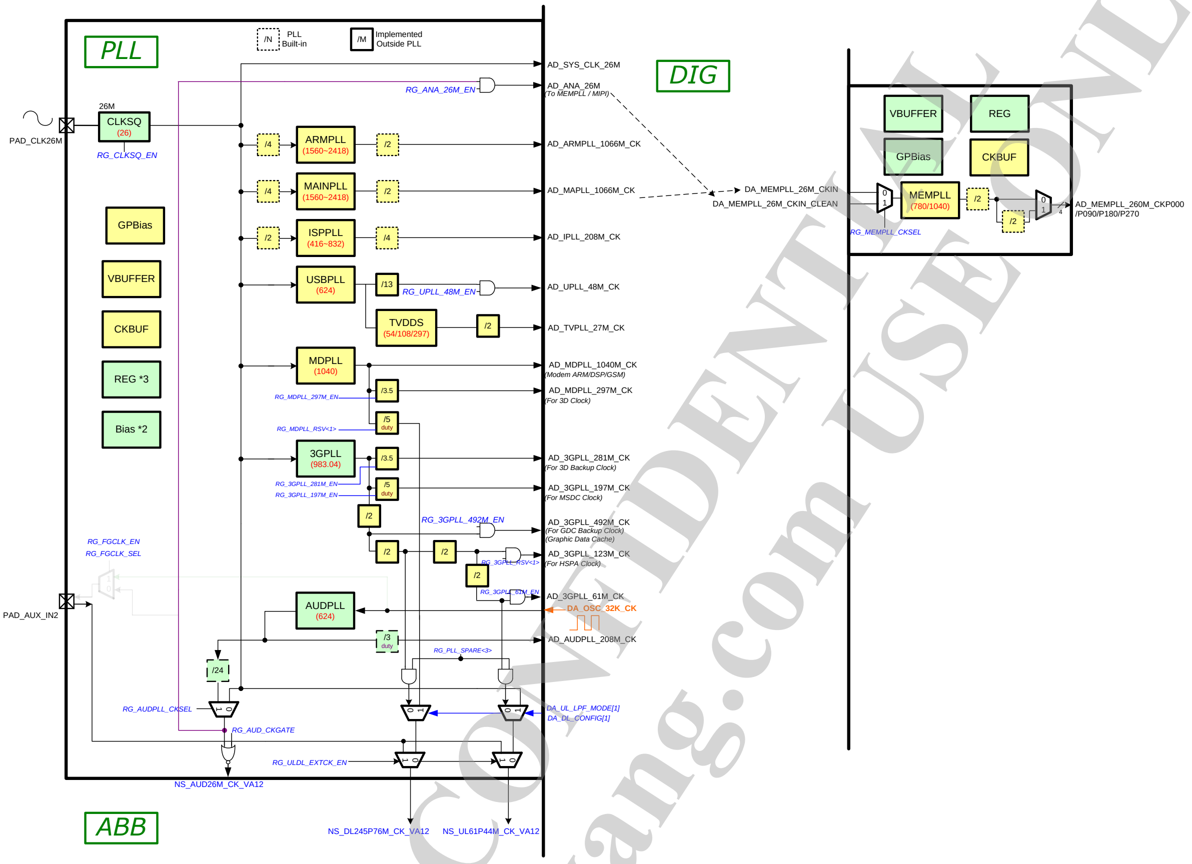

Figure 2-18: Block diagram of PLL.

2.5.10.2 Functional Descriptions

See the table below for the function specifications of PLL.

Table 2-20: ARMPLL specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	780		1209	MHz
	Settling time		30	60	Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	1.0	1.1	1.2	V
AVDD	Analog power supply1 Analog power supply2	2.4 1.7	2.5 1.8	2.6 1.9	V
T	Operating temperature	-20		80	℃
	Current consumption		1		mA
	Power down current consumption			1	uA

Table 2-21: MAINPLL specifications.

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Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	780		1209	MHz
	Settling time		30	60	us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	1.0	1.1	1.2	V
AVDD	Analog power supply1 Analog power supply2	2.4 1.7	2.5 1.8	2.6 1.9	V
T	Operating temperature	-20		80	℃
	Current consumption		1		mA
	Power down current consumption			1	uA

Table 2-22: ISPPLL specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	104		208	MHz
	Settling time		30	60	us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		200		ps
DVDD	Digital power supply	1.0	1.1	1.2	V
AVDD	Analog power supply1 Analog power supply2	2.4 1.7	2.5 1.8	2.6 1.9	V
T	Operating temperature	-20		80	℃
	Current consumption		1		mA
	Power down current consumption			1	uA

Table 2-23: MDPLL specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	1040	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		110		ps
DVDD	Digital power supply	1.0	1.1	1.2	V
AVDD	Analog power supply1 Analog power supply2	2.4 1.7	2.5 1.8	2.6 1.9	V
T	Operating temperature	-20		80	℃
	Current consumption		2		mA
	Power down current consumption			1	uA

Table 2-24: USBPLL specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	624	N/A	MHz

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	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		200		ps
DVDD	Digital power supply	1.0	1.1	1.2	V
AVDD	Analog power supply1 Analog power supply2	2.4 1.7	2.5 1.8	2.6 1.9	V
T	Operating temperature	-20		80	℃
	Current consumption		2		mA
	Power down current consumption			1	uA

Table 2-25: 3GPLL specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	491.52	N/A	MHz
	Settling time		30		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		150		ps
DVDD	Digital power supply	1.0	1.1	1.2	V
AVDD	Analog power supply1 Analog power supply2	2.4 1.7	2.5 1.8	2.6 1.9	V
T	Operating temperature	-20		80	℃
	Current consumption		2		mA
	Power down current consumption			1	uA

Table 2-26: AUDPLL specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	208	N/A	MHz
	Settling time		10		ms
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		200		ps
DVDD	Digital power supply	1.0	1.1	1.2	V
AVDD	Analog power supply1 Analog power supply2	2.4 1.7	2.5 1.8	2.6 1.9	V
T	Operating temperature	-20		80	℃
	Current consumption		1		mA
	Power down current consumption			1	uA

Table 2-27: TVDDS specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		624		MHz
Fout	Output clock frequency	27	54	148.5	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		200		ps
DVDD	Digital power supply	1.0	1.1	1.2	V

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AVDD	Analog power supply1 Analog power supply2	2.4 1.7	2.5 1.8	2.6 1.9	V
T	Operating temperature	-20		80	℃
	Current consumption		2		mA
	Power down current consumption			1	uA

Table 2-28: MEMPLL specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	195	390	520	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	1.0	1.1	1.2	V
AVDD	Analog power supply1 Analog power supply2	2.4 1.7	2.5 1.8	2.6 1.9	V
T	Operating temperature	-20		80	℃
	Current consumption		2		mA
	Power down current consumption			1	uA

2.5.11 32KHz Crystal Oscillator

2.5.11.1 Block Descriptions

The low-power 32 kHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768 kHz crystal and a load composed of two functional capacitors. See the figure below.

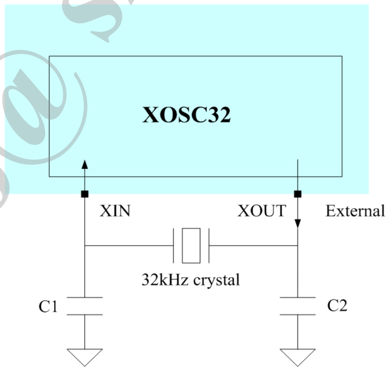

Figure 2-19: Block diagram of 32 kHz crystal oscillator.

2.5.11.2 Functional Descriptions

See the table below for the function specifications of temperature sensor.

Table 2-29: 32 kHz crystal oscillator specifications.

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Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDDRTC	Analog power supply	1.0	2.8	3.0	V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	35	50		%
	Current consumption			5	uA
	Leakage current		1		uA
T	Operating temperature	-20		80	°C

Here are a few recommendations for the crystal parameters used with XOSC32.

Table 2-30: Recommended parameters of 32 kHz crystal oscillator.

Symbol	Parameter	Min.	Typ.	Max.	Unit
F	Frequency range		32,768		Hz
GL	Drive level			5	uW
Δf/f	Frequency tolerance		+/- 20		ppm
ESR	Series resistance			50	KΩ
C0	Static capacitance			1.6	pF
C1(C1/C2in the figure)	Load capacitance	6		12.5	pF

2.5.12 Temperature Sensor

2.5.12.1 Block Descriptions

In order to monitor the temperature of CPU, a temperature sensor is provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

2.5.12.2 Functional Descriptions

See the table below for the function specifications of temperature sensor.

Table 2-31: Temperature sensor specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.16		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C
	Active current		300		uA
	Quiescent current		3		uA

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2.5.13 SIM Interface

2.5.13.1 Block Descriptions

There are two SIM card interface modules to support two SIM cards simultaneously. The SIM card interface circuitry meets all ETSI and IMT-2000 SIM interface requirements. It provides level shifting needs for low voltage GSM controller to communicate with either 1.8V or 3V SIM cards. All SIM cards contain a clock input, a reset input, and a bi-directional data input/output. The clock and reset inputs to SIM cards are level shifted from the supply of digital IO of baseband to the SIM supply (VSIM). The bi-directional data bus is internal pull high to VSIM via 5KΩ resistor.
The 2nd SIM card interface can be used for supporting another SIM card or mobile TV. The interface pins such as SIO2, SRST2, SCLK2, can be configured as GPIO when there is no need to use the 2nd SIM card interface.
All pins that connect to the SIM card (VSIM, SRST, SCLK and SIO) withstand over 5kV HBM (human body mode) ESD. In order to ensure proper ESD protection, careful board layout is required.

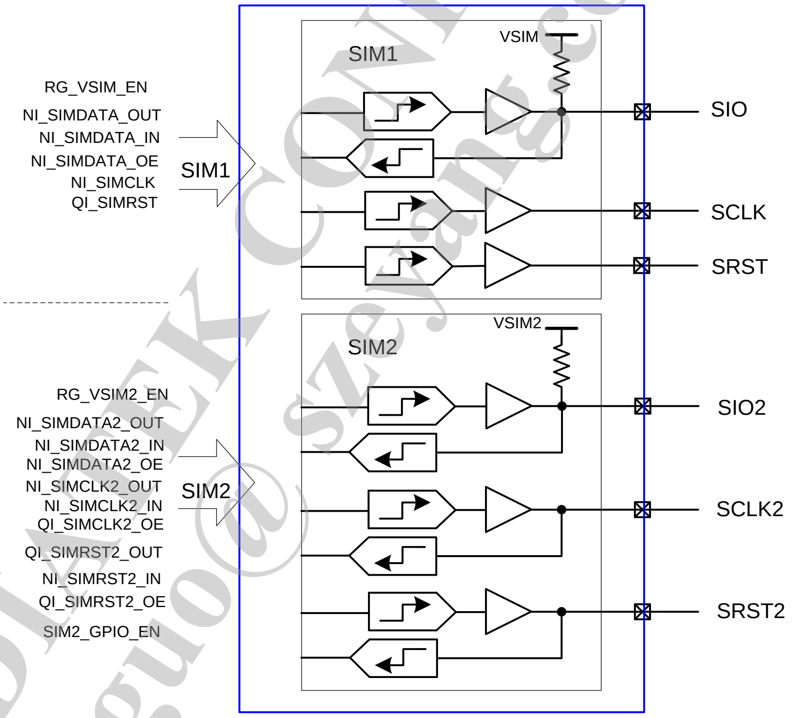

Figure 2-20: Block diagram of SIM interface.

2.5.13.2 Functional Descriptions

See the table below for the function specifications of SIM interface.

Table 2-32: SIM interface specifications.

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Description	Condition	Min.	Typ.	Max.	Unit
Interface to 3V SIM Card					
Output Low of SRST	I = 200 µA			0.36	V
Output High of SRST	I = -200 µA	0.9*VSIM			V
Output Low of SCLK	I = 200 µA			0.4	V
Output High of SCLK	I =-100 µA	0.9*VSIM			V
Input / Output Low of SIO	I=-1mA			0.4	V
Input / Output High of SIO	I = ±20 µA	VSIM-0.4			V
(Iil)Pull high current of SIO	Vil = 0 V			-1	mA
Interface to 1.8V SIM Card					
Output Low of SRST	I = 200 µA			0.2*VSIM	V
Output High of SRST	I = -200 µA	0.9*VSIM			V
Output Low of SCLK	I = 200 µA			0.12*VSIM	V
Output High of SCLK	I = -100 µA	0.9*VSIM			V
Input / Output Low of SIO	I=-1mA			0.15*VSIM	V
Input / Output High of SIO	I = ±20 µA	VSIM-0.4			V
(Iil)Pull high current of SIO	Vil = 0 V			-1	mA
SIM Card Interface Timing					
SIO pull-up resistance to VSIM		4	5	6	kΩ
SRST, SIO rise/fall times	VSIM = 3, 1.8V, load with 30 pF			1	µs
SCLK rise/fall times	VSIM = 3V, CLK load with 30 pF			18	ns
	VSIM = 1.8V, CLK load with 30 pF			50	ns
SCLK frequency	CLK load with 30 pF			5	MHz
SCLK duty cycle	SIMCLK Duty = 50%, fsimclk = 5 MHz	47		53	%

2.5.14 MIPI

Consult the *MIPI Camera Interface Specification (CSI-2 V1.0) and Display Interface Specification (DSI, DPI-2, DPI-2, please see http://www.mipi.org/specifications)* for more information on MIPI usage and requirements.

2.5.15 USB2.0

Consult the *Universal Serial Bus Specification*, Revision 2.0 (see www.usb.org/developers) for more information on USB usage and requirements.

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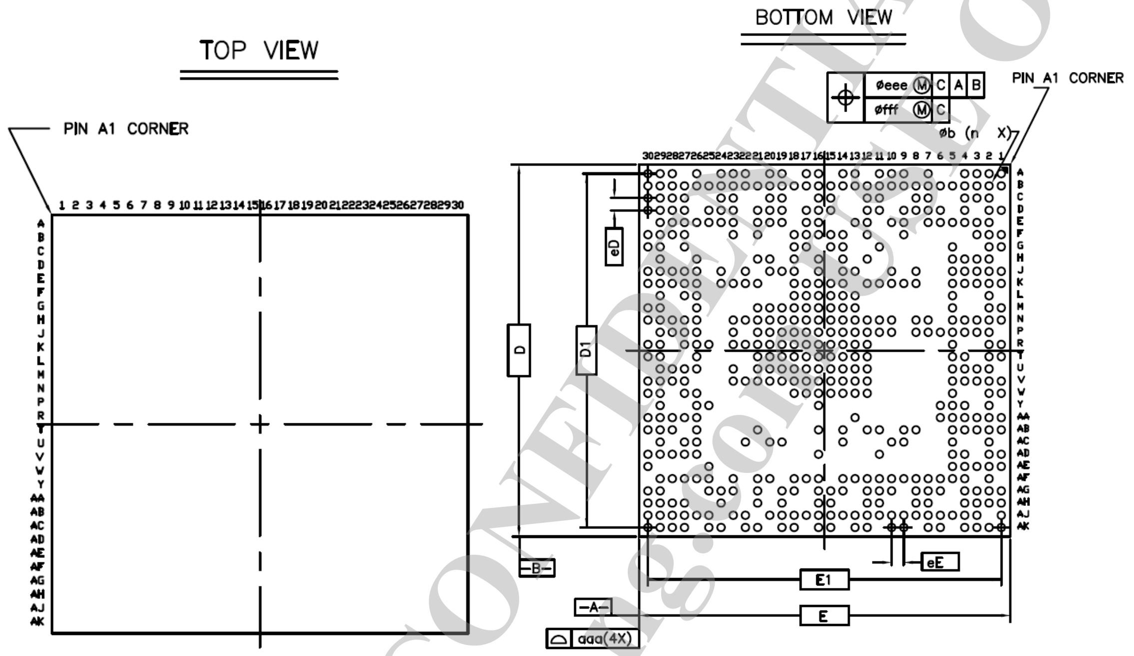
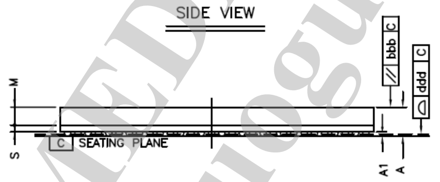
2.6 Package Information

2.6.1 Package Outlines





		Symbol	Common Dimensions
Package :			TFBGA
Body Size:	X	E	12.200
	Y	D	12.200
Ball Pitch :	X	eE	0.400
	Y	eD	0.400
Total Thickness :		A	1.200 MAX.
Mold Thickness :		M	0.700 Ref.
Substrate Thickness :		S	0.260 Ref.
Ball Diameter :			0.250
Stand Off :		A1	0.110 ~ 0.210
Ball Width :		b	0.200 ~ 0.300
Package Edge Tolerance :		aaa	0.100
Mold Flatness :		bbb	0.100
Coplanarity:		ddd	0.080
Ball Offset (Package) :		eee	0.150
Ball Offset (Ball) :		fff	0.050
Ball Count :		n	537
Edge Ball Center to Center :	X	E1	11.600
	Y	D1	11.600

Figure 2-21: Outlines and dimensions of TFBGA 12.2mm*12.2mm, 537-ball, 0.4mm pitch package.

2.6.2 Thermal Operating Specification

Table 2-33: Thermal operating specification.

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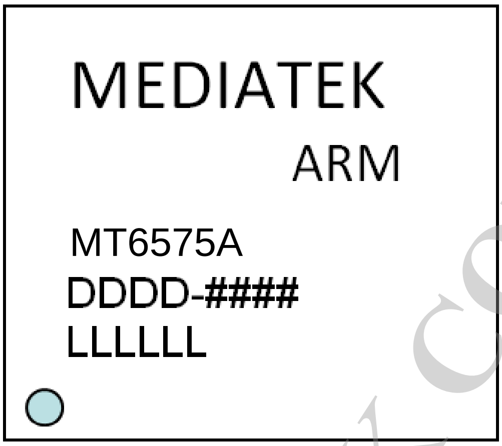
Symbol	Description	Value	Unit	Notes
	Maximum operating junction temperature	125	°C	
	Package thermal resistances	7.5	°C/Watt	
	Package thermal resistances in nature convection	31.54	°C/Watt	

2.6.3 Lead-free Packaging

MT6575 is provided in a lead-free package and can meet RoHS requirements.

2.7 Ordering Information

2.7.1 Top Marking Definition



MT6575A : Part No
DDDD : Datecode
: Subcontractor code
LLLLLL : Die Lot Number

Figure 2-22: Top mark of MT6575.

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